

PathWave Design Software

THE NEXT GENERATION OF ELECTRONIC DESIGN AUTOMATION



For more information:

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Introduction

Gone are the days of simple design. Every year, designers push new limits: longer battery life, smaller components, higher levels of integration.

With complex design comes new challenges. Designers spend hours setting up and running simulations. Mountains of data wait to be measured and analyzed. Engineers need to create workarounds to connect multiple design tools. Meanwhile, wireless standards are evolving quickly. To keep up with the strong demands of modern technology, designers need a new approach.

The Next Generation of Electronic Design and Test

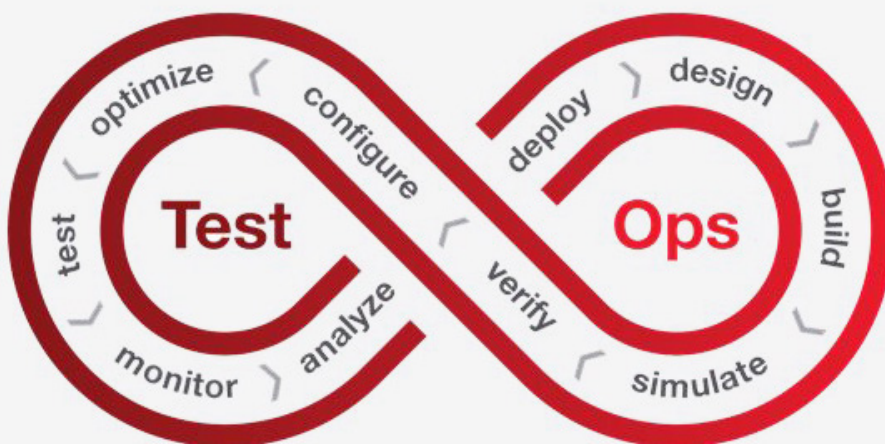
Connected, agile design and test is a transformational way to approach the development of electronic systems. It combines new software, new workflows, and powerful automation tools in a way that transforms legacy processes and yields substantial productivity and equipment utilization improvements.

The approach moves organizations from siloed design and test steps to agile, connected workflows. The benefits mirror those of agile software design and DevOps: faster device design, translation of design parameters into test requirements, and execution and validation of test results. When coupled with automation, what results is a new development culture known as TestOps. (Read more in [The TestOps Manifesto: A Blueprint for Connected, Agile Design and Test](#).)



Achieving a TestOps environment requires changes in process, tools, and culture. With the right tools and processes in place, measurable improvements in three critical areas can be realized:

- Reduced engineering time.
- Improved equipment utilization.
- Improved throughput.



The Transformation Starts with Design

There is tremendous opportunity to reduce time-to-market across the design and simulation phases of the electronic product development lifecycle. Most challenges slowing the lifecycle today can be distilled down to data movement and tool integration. Information sharing across the workflow is one of the biggest challenges for design and test engineers. In fact, **9 out of 10 companies revealed** that correlating test result data with simulation takes months.

The reason data correlation takes so long is primarily because of the numerous tools used throughout the development lifecycle. Over **50% of designers** use more than 5 different tools for simulation and design. The software tools are not integrated and require hours of coding each week to enable data sharing. The magnitude of that integration effort is amplified by the fact that nearly every company is devoting more resources to the maintenance of in-house tools. Designers are looking for an integrated solution that leverages shared data to accelerate their electronic design.

PathWave Design Software

PATHWAVE

Keysight's PathWave Design software is a collection of electronic design automation software tools that accelerates product development by reducing the time engineers spend in the design and simulation phase. Its libraries and customized simulators reduce setup time. The software seamlessly integrates circuit design, EM simulation, layout capabilities, and system level modeling, reducing time spent in importing and exporting designs and fixing errors associated with changing tools. Improvements in data analytics allow for faster analysis and more timely design decisions. Automation improvements reduce manual work.

The latest collection of releases, PathWave Design 2020, provides engineers with new tools and software enhancements to bring efficiencies into their RF and microwave, 5G, and automotive design flows, shortening the design cycle and reducing project delays.

PathWave Design 2020 delivers:

- Enhanced performance
- Improved data analytics
- Revolutionary new design workflows
- Connected circuit and EM simulation

PathWave Design Accelerates Workflows in 5 Key Industry Segments:

RF & Microwave Solutions

Today's RF & microwave designs require multi-chip modules with more elaborate interconnects and packaging. Complexity in electronic design is increasing. 5G requires higher frequencies and broader modulation bandwidth. There is more simulation and measurement data to analyze than ever before. Despite these time-consuming challenges, designers are often pressured to accelerate their time-to-market to stay ahead of the competition.



CHALLENGE 1: Designers struggle to connect multiple software tools

Designers typically use more than one design software to design and simulate their devices. Most of the time, they are forced to create manual workarounds so that the different software tools can communicate. Additionally, their EM simulators and circuit simulators are different. They perform each simulation separately and then compare the data from the different tools. The time spent importing, exporting, and error-checking slows designers down and significantly impacts overall time-to-market.

Keysight PathWave Design offers a variety of solutions for RF & microwave designers looking to speed their design workflow and bring products to market more quickly and efficiently.

SOLUTION: PathWave Advanced Design System (ADS)

Performing circuit analysis on multiple devices can be time consuming and difficult. **PathWave Advanced Design System (ADS)** is Keysight's leading RF, microwave, signal integrity, and power integrity design platform. With multiple libraries, bundles, design guides, and simulation elements, PathWave ADS is the one software tool to help you overcome any design challenge.

PathWave ADS provides a complete, integrated set of easy-to-use 3D EM circuit and system simulators. Designers can perform EM and circuit co-simulation in one single tool. PathWave ADS combines schematic, layout, circuit, electro-thermal co-simulation and three full-wave 3D EM technologies with integrated circuit (IC), package, laminate, PCB, and 3D EM component co-design in one software tool to dramatically improve productivity and reduce cost.



New Features In PathWave ADS 2020:

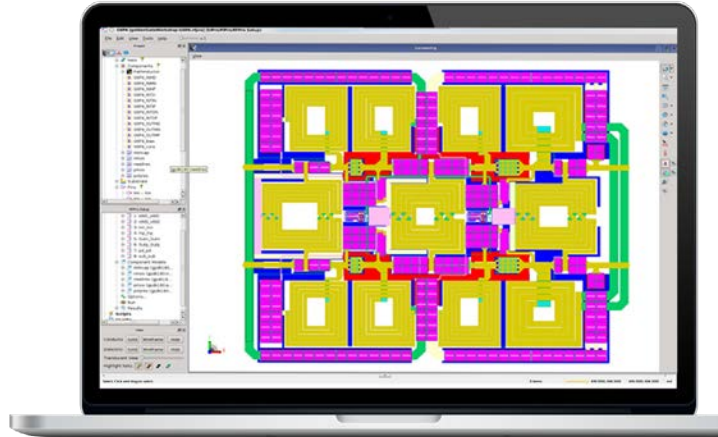
- 5G Virtual Test Benches updated with the latest 5G NR Tests
- Improved workspace management tools
- Stackable PCB VIAs
- New EM simulator for RF Circuit Design, RFPro
- New EM Simulator for Power Electronics, PEPro



SOLUTION: RFPro in PathWave Advanced Design System (ADS)

RFPro is the next generation EM simulator for RF and microwave circuit designs. RFPro revolutionizes RFIC, MMIC & RF module design for 5G wireless, aerospace/defense, automotive, and IoT applications by seamlessly integrating EM with circuit simulation. It is industry's first EM simulation platform dedicated to RF/microwave circuit designs.

Seamlessly integrated with PathWave ADS, RFPro makes performing EM analysis as easy as running circuit simulations. The predictive expert settings are like having a dedicated EM simulation expert just for your design.

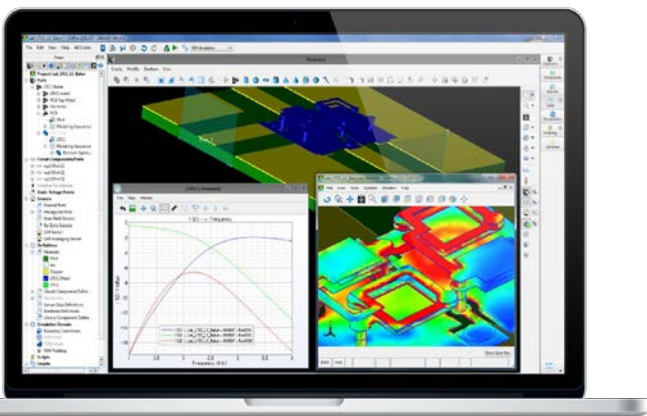


RFPro In PathWave ADS Key Benefits:

- Instant EM access during design with a single integration into PathWave ADS & Cadence Virtuoso
- Automatic EM expert settings guarantee confidence in EM results for novice and expert users
- Fast & correct analysis setup, regardless of problem size for quick, interactive EM and EM-circuit co-simulation on demand
- Enhanced MoM and FEM simulator performance

SOLUTION: PathWave EM Design (EMPro)

PathWave EM Design (EMPro) is an EM simulation design platform for analyzing the 3D EM effects of components such as high-speed and RF IC packages, bondwires, antennas, on-chip and off-chip embedded passives, and PCB interconnects. RF board designs include 3D components and connectors that need to be characterized to high frequencies. Component and connector designs created in other CAD tools can be imported into PathWave EM Design (EMPro). They can then be simulated using either Finite Element Method (FEM) or Finite Difference Time Domain (FDTD) simulation technology.



High-frequency components are sensitive to interactions with surrounding PCB traces and vias. These 3D components can be created and simulated in PathWave EM Design (EMPro), and then combined with a board layout in PathWave ADS for complete 3D EM simulation using FEM technology.

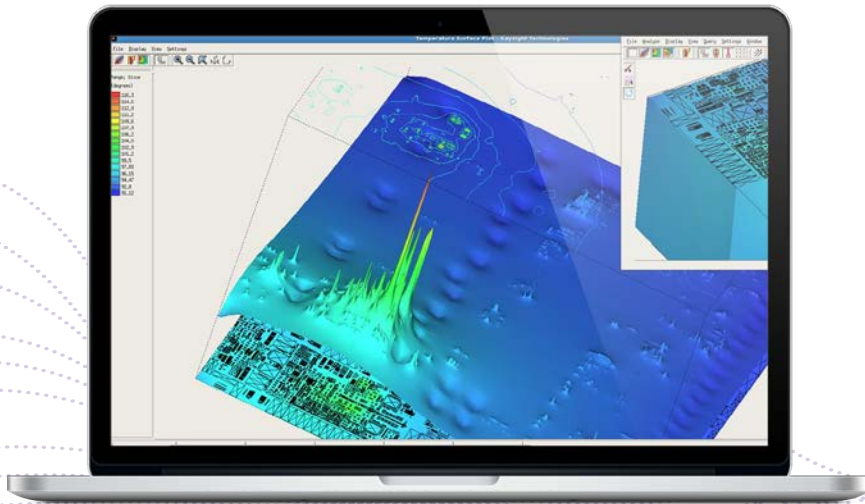


PathWave EM Design (EMPro) Key Benefits:

- 3D solid modeling environment
- Speeds design with integration into PathWave ADS
- Time and frequency domain simulation

SOLUTION: PathWave Thermal Design

High performance ICs have areas with very high-power density, causing excessive temperature variations. **PathWave Thermal Design** is a device-level electro-thermal simulator for ICs and stacked-die SiP. It computes a 3D temperature profile of your chip and inputs the thermal analysis data into your circuit simulator. Your circuit simulator will show how temperature affects your circuit's performance, helping neutralize adverse temperature effects before committing to fabrication. By providing the accurate operational temperature profile within the IC, users can discover hotspots and excessive temperature variations in precision circuitry. PathWave Thermal Design works with several IC design tools, including Cadence Virtuoso.



PathWave Thermal Design Key Benefits:

- High capacity: can handle large-scale analog/mixed-signal and digital IC designs
- High precision: provides accurate, device-level temperature data at sub-micron resolution
- Electrothermal solver works with your circuit simulator to provide temperature-aware simulation results

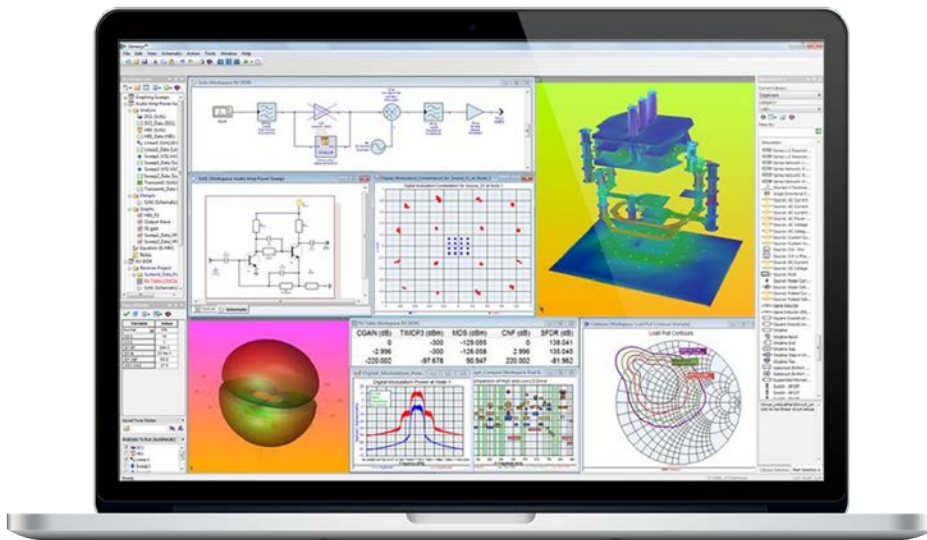
CHALLENGE 2: RF board designs are increasing in complexity

Designing circuits with discrete resistors, inductors, and capacitors can be a tricky problem for RF design engineers. Simple software tools can only calculate ideal inductor and capacitor values. Since real-world discrete components are not ideal, their actual performance does not entirely match the theoretical performance of the ideal parts. Real-world discrete components contain parasitics that affect their performance.

When considering real-world performance, designers quickly realize that RF circuit design is not a straightforward process. Obtaining desired results comes at the expense of a long and difficult trial-and-error process in the lab. To overcome these challenges, designers need software that can help them save time and effort when designing circuits with discrete resistors, inductors, and capacitors.

SOLUTION: Keysight PathWave RF Synthesis (Genesys)

PathWave RF Synthesis (Genesys) is an affordable, accurate, easy-to-use RF and microwave circuit synthesis and simulation tool created for the circuit board and subsystem designer. Automatic circuit synthesis of matching networks, filters, oscillators, mixers, transmission lines, PLL and signal routing structures enable engineers without prior expertise to design these components quickly.



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PathWave RF Synthesis (Genesys) Key Benefits:

- Industry's widest coverage of RF and microwave automatic circuit synthesis
- Comprehensive RF system architecture
- 3D-planar EM simulation
- Time and frequency domain simulation
- X-parameter* nonlinear circuit and system simulation

*X-parameters is a trademark and registered trademark of Keysight Technologies in the US, EU, JP, and elsewhere. The X-parameters format and underlying equations are open and documented. For more information, visit <http://www.Keysight.com/find/eesof-x-parameters-info>

CHALLENGE 3: RF and IC designers need similar methodologies and design tools

The increasing complexity and performance demands on analog and mixed-signal RFICs challenge the RFIC designer to adopt tools with ever increasing levels of performance and flexibility. Physical effects enormously complicate the design and require a solution that brings together the best EDA tools in one seamless design flow. Historically, IC and RF designers have used different design methodologies and tools. With IC applications approaching several GHz, silicon is bridging the gap between traditional low-frequency analog design and discrete RF design. Designers need a standard tool that can do both IC and RF accurately.

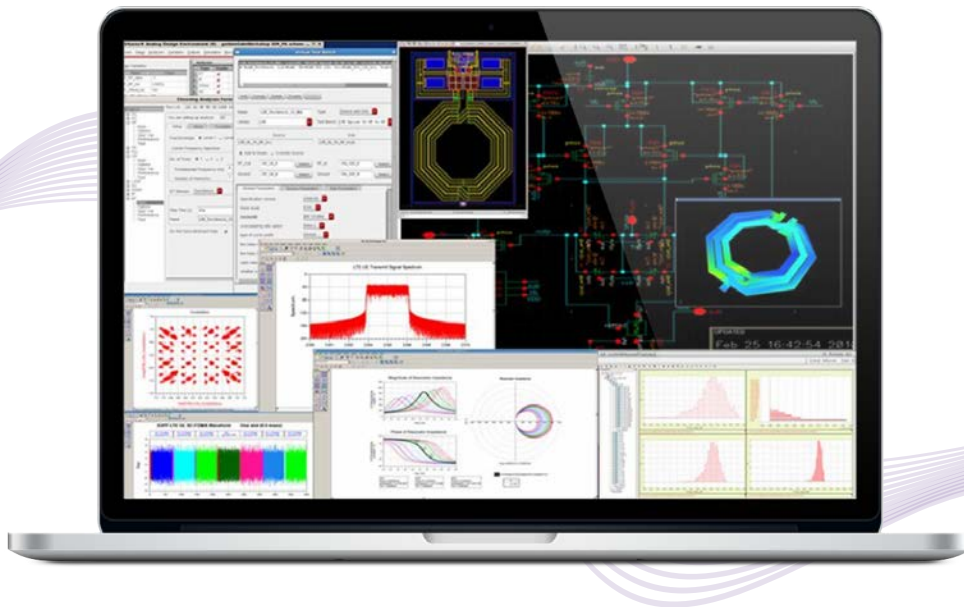
SOLUTION: PathWave RFIC Design (GoldenGate)

PathWave RFIC Design (GoldenGate) is an advanced simulation and analysis solution for integrated mixed signal RFIC designs that is fully integrated into the Cadence Analog Design Environment (ADE). It provides the framework for RFIC designers to rapidly simulate circuits, verify specifications, and validate potential yield of complex highly integrated devices. Designers can analyze circuit manufacturability using industry standard techniques such as Monte Carlo, as well as unique Keysight statistical mismatch and process analyses.

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PathWave RFIC Design (GoldenGate) Key Benefits:

- Best-in-class RF circuit simulator
- Advanced analysis support
- Automation and usability
- RF to mmWave design support
- Wireless standard-compliant design capability





High-Speed Digital Design Solutions

High-speed digital standards are quickly evolving to keep pace with emerging technologies such as 5G, internet of things (IoT), artificial intelligence (AI), virtual reality (VR), and autonomous vehicles. Each generational change of high-speed computing standards provides new features and faster data transfer rates, creating new design challenges. Faster speeds require high-speed precision testing and validation of compliance to the latest standards.

To support the explosion of data center traffic, new digital standards are rapidly increasing in speed, while cost pressures remain the same. Signal and power integrity engineers must work to ensure that devices operate reliably, and chip-to-chip links deliver the desired bit error rate (BER) for the system. To counter high signal loss in PCBs, designers are exploring new technologies like complex equalization training and multi-level signaling (PAM-4).



CHALLENGE 1: New standards bring faster speeds and more factors to consider

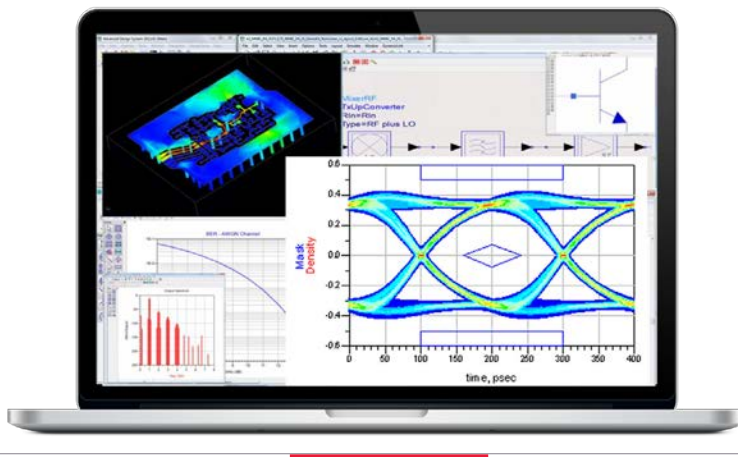
Designers are using new sophisticated algorithms to improve signaling interfaces for high-speed digital designs. Even so, it is difficult to compensate for die, package, and PCB parasitics. There is an increasing need to design controlled-impedance transmission lines, including modeling via effects to avoid interface failure. IC failures are increasing due to signaling noise in ground and power planes.

Transmission lines and via transitions form the high-speed signal path between a transmitter and a receiver. These paths are known as PCB interconnects, and if not optimally designed they can easily destroy the signal integrity of a link. The amount of signal distortion can be seen in an eye diagram. An open eye corresponds to minimal signal distortion, but loss and reflections in the system can cause the eye to close, corresponding to distortion of the signal.

SOLUTION: Channel Simulation in PathWave Advanced Design System (ADS)

The PathWave Advanced Design System (ADS) Channel Simulator first became prevalent when transient simulation (SPICE) couldn't address the measurement of margin-to-mask for low BER, as demanded by high-speed link designs. It continues to be the industry standard for channel simulation today. Keysight's **W2308EP Channel Simulator Element** has the widest range of vendor transmit/receive models. It ensures S-parameter models are handled accurately in simulation with proprietary algorithms.

PathWave ADS has tools for all your pre-layout design exploration challenges. You can calculate line impedances with the Controlled Impedance Line Designer and model via behavior with the Via Designer. You can optimize link performance with integrated circuit optimization. You can even understand where the signal is degraded with integrated time-domain reflectometry (TDR) analysis. With all of these tools you will be able to minimize impedance mismatches and improve your margins.



Channel Simulation in PathWave ADS Key Benefits:

- Complete chip-to-chip link analysis
- Eye diagram analysis including BER contour and bathtub display
- Equalizer support with automatic tap optimization
- Ability to check crosstalk with multiple aggressors each at different data rates
- Correct treatment of jitter amplification

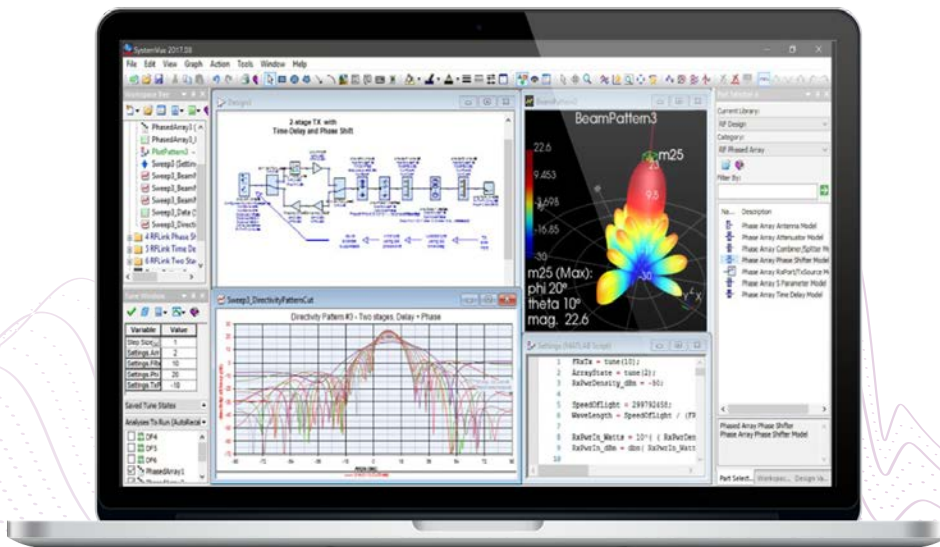
SOLUTION: PathWave System Design (SystemVue)

One of the ways that the electronics industry has dealt with the increasing demand for data communication throughput between system components is a new modeling approach – the input/output buffer information specification-algorithmic modeling interface (IBIS-AMI). **PathWave System Design (SystemVue)** is a focused electronic design automation (EDA) environment for electronic system-level (ESL) design, offering automated AMI-model generation in its **W1714EP AMI Modeling Kit**. You can use it to automate code-generation and model compilation within minutes. PathWave System Design (SystemVue) offers the basic building blocks to jumpstart model development. You can easily customize models to include custom intellectual property (IP) and build systems confidently knowing that you are using industry-validated modeling technology. Then, with PathWave ADS, you can accurately simulate complex signal links with jitter, equalization, and clock and data recovery with the channel simulator and IBIS-AMI models.



IBIS-AMI Modeling with PathWave System Design (SystemVue) Key Benefits:

- Automate AMI-model generation in minutes
- Customize models to include custom IP
- Gain confidence with industry-validated modeling technology
- Jumpstart development with basic building blocks



CHALLENGE 2: Designs need to meet electromagnetic inference and compliance regulations

Electromagnetic emissions from a device or system that interfere with the normal operation of another device or system is known as electromagnetic interference (EMI). A system's ability to operate without introducing intolerable electromagnetic disturbance is known as electromagnetic compliance (EMC). EMI and EMC are not new issues for system engineers. However, with increasing data rates in computers, networks, storage and mobile devices, design engineers are more challenged to deal with not only the traditional emissions issues, but also coupling issues with nearby circuit and system components. Designers need a way to ensure their devices meet EMI and EMC regulations.

SOLUTION: PathWave EM Design (EMPro)

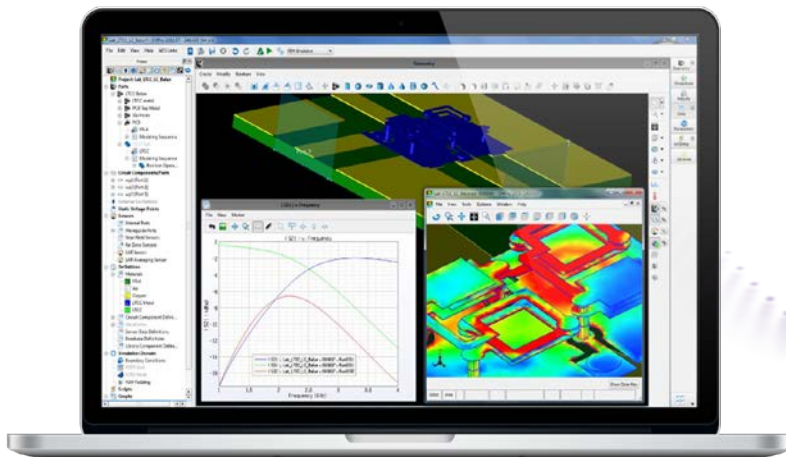
PathWave EM Design (EMPro) provides the flexibility of drawing arbitrary 3D structures and the convenience of importing existing CAD files. You can create 3D shapes, add material properties, set up simulations, and view results—all within the EM environment. Before building your PCB, you can run electromagnetic interference/compliance (EMI/EMC) tests with the solver and the emission calculator. You can also run electrostatic discharge (ESD) analysis with standard-compliant waveforms.

One of the issues designers face with EMC and EMI is interference between subsystems and antennae. It is an especially severe problem in mobile devices, where designs are squeezed into very small areas. The interference can cause degradation in receiver sensitivity, also known as “RF de-sense” or “RFI” issues. With PathWave ADS and EM Design, you can model EM field interactions within devices and handle digital waveforms from circuit and system-level design tools. You can also simulate the radiated emissions of electronic circuits and components and determine whether these emissions are within levels specified by common standards and compliant—all before hardware has been developed.



PathWave EM Design (EMPro) for EMI/EMC Key Benefits:

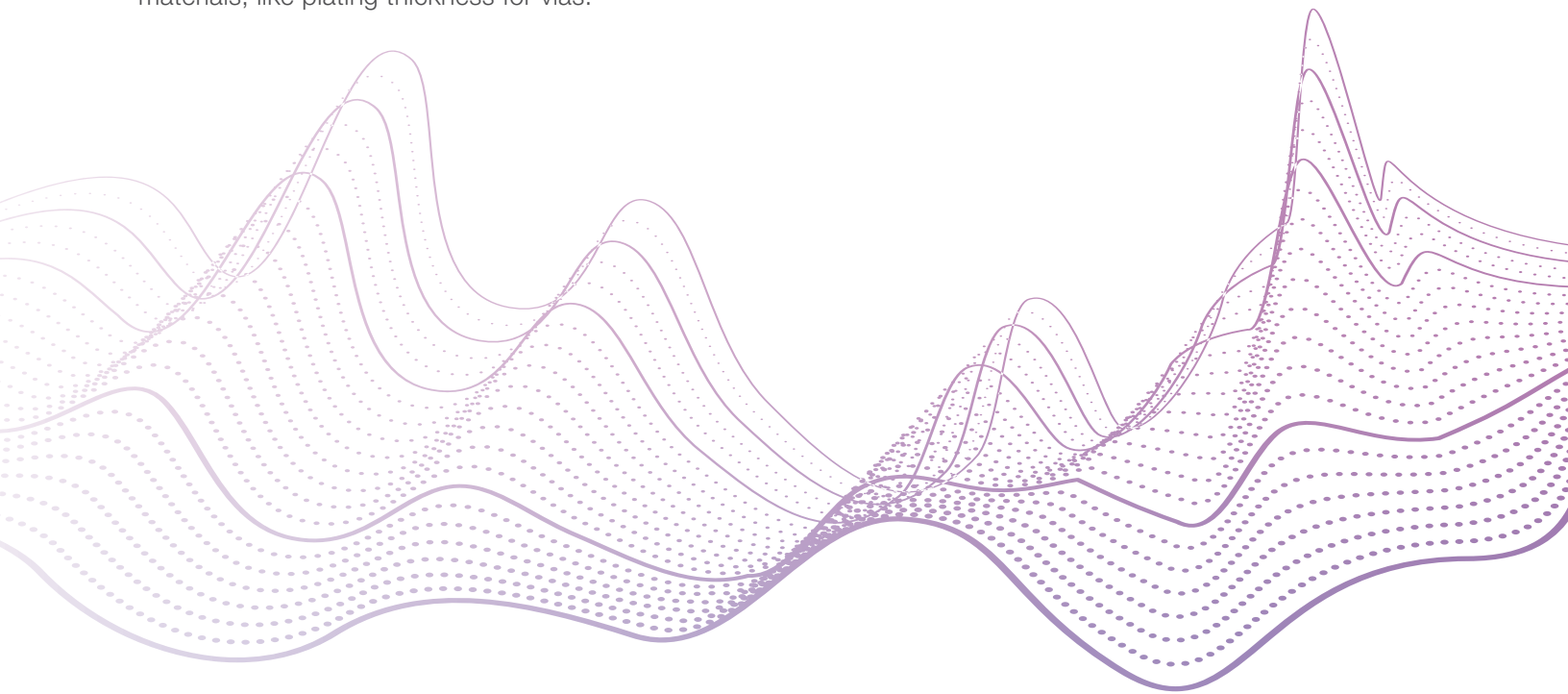
- Run EMI/EMC test before building your PCB
- Run ESD analysis with standard-compliant waveforms
- Address “RF de-sense” or “RFI” issues
- Access standard, user-defined, and measured waveforms



CHALLENGE 3: Perform signal and power integrity analysis with accuracy in a reasonable amount of time

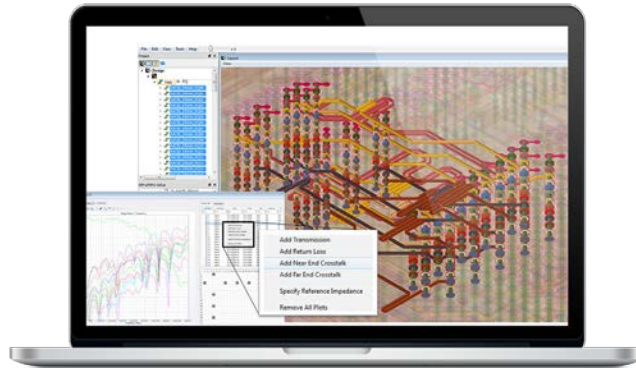
EM technologies are typically used to accurately characterize loss and coupling of high-speed channels. As data rates increase, a major dilemma is the choice of which EM technology to use. Full-wave general purpose EM simulation tools offer accuracy at high-frequencies. The limiting factor of 3D EM technology for signal integrity analysis is simply the scale and complexity of PCB designs. Densely-routed boards require hours of engineering time to manually simplify a layout, cookie-cut the signal nets, and optimize meshing to achieve accurate results in a practical time (many hours of simulation). Designers can only verify small sections of the board at one time. Hybrid simulators are much faster by comparison and can be used for greater coverage of the nets on the boards; however, there is always the question of whether or not the simulation correlates well with measurement. Moreover, the designer is left wondering what EM effects were missed by using the simplified techniques?

Power integrity (PI) has become an ever-increasing challenge in modern high-speed systems, driven by two main forces: higher device integration with lower IC supply voltages and shrinkage of the PCB for small form factors. Because of this, a true power integrity – direct current (PI-DC) simulator is required to consider the real physical layout of the power delivery network (PDN), together with inputs for materials, like plating thickness for vias.



SOLUTION: SIPro in PathWave Advanced Design System (ADS)

SIPro Signal Integrity EM Analysis Element provides signal integrity (SI) analysis of your high-speed PCBs, enabling you to characterize loss and coupling of signal nets, and extract an EM-accurate model that can be used in the PathWave ADS Transient and Channel Simulators. From the net-driven user interface—a feature common to both SIPro and PIPro—designers can quickly select only those nets they want to simulate, together with the power and ground planes and components, and with no time or engineering effort required to manually edit or manipulate layout objects before simulation. Ports can also be automatically setup. With this workflow, designers can go from layout to results in less than 20 clicks.



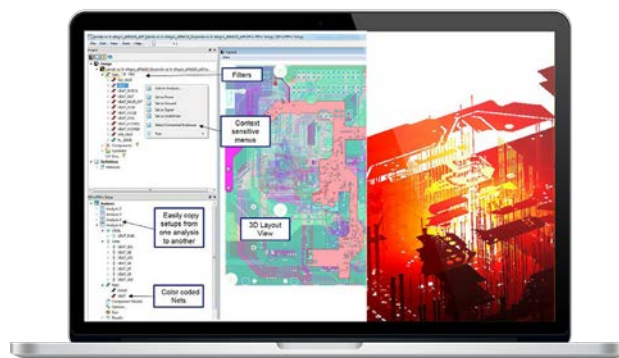
SIPro in PathWave ADS Key Benefits:

- Fast and accurate simulation of large, complex PCB designs
- Layout to results in less than 20 clicks
- Innovations in EM-Mesh Domain Optimization
- Complete channel analysis
- EM model extraction

SOLUTION: PIPro in Pathwave Advanced Design System (ADS)

PIPro Power Integrity EM Analysis Element provides power integrity analysis of your power distribution network (PDN), including DC IR drop analysis, AC impedance analysis, and power plane resonance analysis. The EM technologies in PIPro are tuned specifically for PI applications; they are much faster and more efficient than general-purpose EM tools. PIPro utilizes a common setup and analysis environment within PathWave ADS.

The PIPro suite of EM simulators offers the perfect solution for considering the real physical layout of the PDN. With a dedicated PI-DC simulator, designers get visual feedback in just seconds on exactly what the voltage distribution looks like for selected power and ground nets.



PIPro in PathWave ADS Key Benefits:

- 3D view of layout, selected nets, ports and components
- DC IR drop analysis
- Power plane resonance analysis and 3D field plots
- Comprehensive results reporting (html and docx formats)

CHALLENGE 4: Memory designs continue to grow in complexity

Double data rate (DDR) memory designs grow more complex with each new generation. Simulation and test configuration also grow in complexity, resulting in longer simulation and test setup times. The added complexity makes it harder to correlate simulation and test data, resulting in less confidence in designs, longer troubleshooting cycles, and missed delivery schedules.

Hardware designers working on memory systems must contend with both shrinking timing and voltage margins, and a complex list of compliance measurements to ensure reliable operation. As we move to DDR4 and beyond, random jitter becomes much more significant. Designers need to have confidence their memory designs can pass receiver mask tests at ultra-low BERs.

SOLUTION: Memory Designer in PathWave Advanced Design System (ADS)

Memory Designer minimizes the engineering effort required to setup and extract EM models, simulate buses, and perform compliance testing. It enables designers to use the same measurement science for both simulation and hardware verification stages. Memory Designer is fully integrated within PathWave ADS with new schematic components for easy setup of controller, PCB, connectors, terminations, and memory.



Memory Designer in PathWave ADS Key Benefits:

- New schematic components
- Faster setup and parameterization
- Automated wiring connections
- DDR Bus simulator to characterize signal integrity
- New Memory Probe
- New strobed-eye diagrams and skew measurements
- Automated DDR4 Compliance Test suite and report generation



Power Electronics Solutions

In contrast to traditional electronics, which is all about handling data, power electronics is all about handling power: generating it, converting it, and moving it from source to load. This technology finds applications in a wide range of industries including power utility generation and distribution, automotive, and consumer electronics.

The need to reduce energy consumption, as well as CO₂ emissions, is driving the growth of power electronics and power converters. Unfortunately, current applications relying on silicon-based power devices are at their limits in terms of conversion efficiency and reliability. The emergence of wide band gap (WBG) power devices based on silicon carbide (SiC) and gallium nitride (GaN) hold great promise for moving beyond these limits.



CHALLENGE 1: Switched-mode power supplies require new thinking about EDA tools

Demand for switched-mode power supplies (SMPS) is driven by the need for greater efficiency, increased power density and lower cost. New semiconducting materials such as silicon carbide (SiC) and gallium nitride (GaN) will power future applications due to their high performance and efficiency. However, high performance materials result in new challenges, as the layout of PCBs becomes more difficult. Post-layout analysis of a “virtual prototype” is ideal for managing this challenge, but it requires expertise with a complicated, general-purpose EM field solver.

The high di/dt edges of modern switched-mode power supplies requires new thinking about EDA tools. Traditional pre-layout SPICE is no longer enough because it doesn't account for the voltage spikes and EMI/EMC issues caused by layout parasitics. A new workflow that adds a post-layout EM-circuit co-simulation stage is needed to find and fix these problems.

SOLUTION: Power Electronics Library in PathWave Advanced Design System (ADS)

The **Power Electronics Library** in PathWave ADS contains components specifically built for power electronics including those for closed loop feedback regulation of SMPS. For example, the pulse width modulator works with both the transient convolution and harmonic balance simulators. The component palette also provides easy access to the built-in components in PathWave ADS, which are often used in power electronics.

The library provides everything power electronics designers need for a complete self-contained workflow for chip, package, and board design. A “virtual prototype” in PathWave ADS can be simulated in both the time- and frequency-domains. You can combine both lumped and distributed elements. With PathWave ADS you can even obtain the periodic steady state solution efficiently.



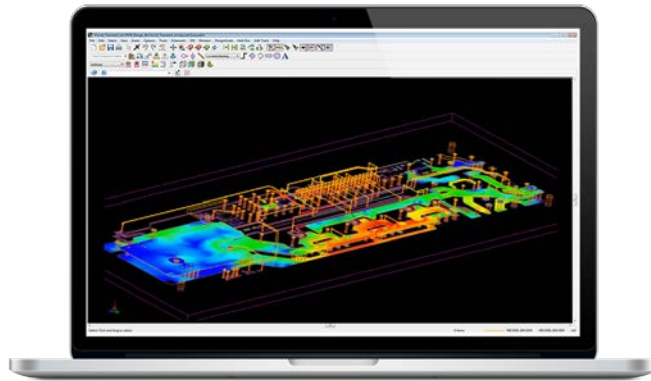
Power Electronics Library in PathWave ADS Key Benefits:

- Cut down on costly, time-consuming board spins
- Analyze design effects without building and testing prototypes
- End-to-end simulation of the complete power ecosystem
- Accurately simulate electromagnetic interference
- Capture analog behavior of logic gates

SOLUTION: PEPro in PathWave Advanced Design System (ADS)

PEPro is the next generation EM-circuit co-simulation platform for SMPS designs. PEPro revolutionizes power converter design for power generation and transmission, aerospace/defense, automotive, data center, consumer electronics, and IoT applications by seamlessly integrating EM with circuit simulation.

PEPro makes performing EM analysis as easy as running circuit simulations, with predictive expert settings that used to require configuration by rare and dedicated EM simulation experts. In addition, it offers pre-built analyses of effects such as voltage spiking and EMI.

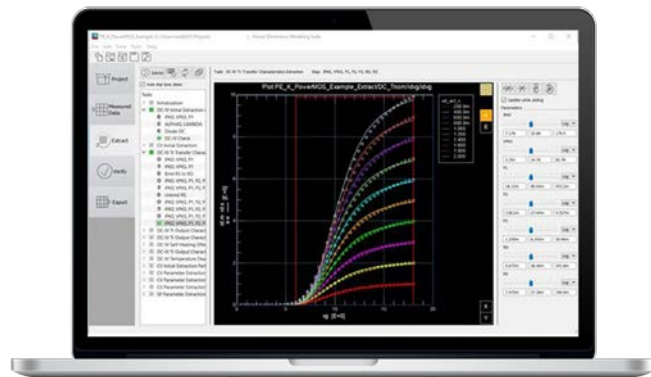


PEPro in PathWave ADS Key Benefits:

- New user interface for easy post-layout analysis
- Automatic optimum settings of EM analysis and simulation controllers
- Analyze, tune, and optimize EM circuit co-simulation
- Visualize current crowding via circuit excitation

SOLUTION: Power Electronics Model in PathWave Device Modeling (IC-CAP)

The **Power Electronics Model** is an advanced device modeling software tool tailored toward the model extraction requirements of discrete semiconductor power electronic devices. It offers device modeling engineers and circuit designers the most advanced and customizable software environment for all modeling needs, including data visualization, simulation, optimization, verification, and reporting. The current version supports simple, fast and highly accurate automated model extraction for a selection of discrete power electronic specific compact and circuit models: GaN high electron mobility transistor (HEMT), Si/SiC Power metal-oxide-semiconductor field-effect transistor (MOSFET), and insulated-gate bipolar transistor (IGBT).



Power Electronics Model in PathWave Device Modeling (IC-CAP) Key Benefits:

- Industry standard ASM-HEMT model support for GaN discrete and IC devices
- Automatic import of measured data (DC, CV, and S-parameters)
- Fast data visualization
- Temperature dependent modeling
- Report generation
- Part of a complete workflow for power electronics design



System-Level Design Solutions

Three application areas driving the need for system designers to use tools that model the increasingly complex RF and baseband interactions in their solutions are: 5G New Radio (NR), aerospace/defense, and autonomous driving. 5G NR development is expanding rapidly into the design phase and co-design of circuit and system is essential to first-pass success. Aerospace/defense electronic warfare innovations require complex signal generation and analysis for multiple emitter scenarios. Autonomous driving sensor integration requires new design approaches for automotive radar to rapidly identify and react to complex driving environments.



CHALLENGE 1: 5G NR designs require end-to-end system verification with digital and RF circuits

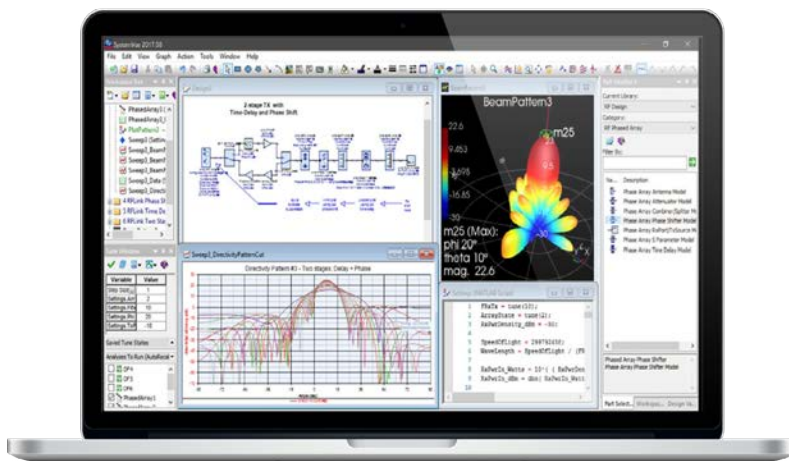
In 5G NR deployment, being late is not an option. Designers are under immense time pressures with 5G technology, development, verification, and deployment all happening in parallel. Designers who do not use a verified reference 5G NR baseband library risk missing specifications. Larger array sizes, bandwidth, frequency, distortion, and modulation complexity found in 5G multiply that risk. Mitigating the challenge requires the use of more sophisticated RF and baseband system simulation earlier in the development process.

One of the key issues in radio interface design for mmWave communications is the selection of the waveform. At high carrier frequencies (e.g., mmWave bands), transmitted and received signals can suffer from severe hardware impairments. Evaluating the performance of several state-of-the-art waveforms in the presence of hardware impairments is of great importance for proper waveform design.

SOLUTION: 5G NR Library in PathWave System Design (SystemVue)

The **5G NR Library** is a trusted reference digital signal processing (DSP) modeling product, supporting the 3GPP standards for the 5G NR physical layer specification. The intellectual property (IP) blocks are cross validated with major 5G chipset makers during the early system modeling and prototyping phase.

With PathWave System Design (SystemVue) you have access to integrate 5G NR baseband IP, various RF transceiver design examples operating in sub-6GHz and mmWave frequency, and phased array and beamforming models using antenna patterns from EM software or measurement. It provides the best system-level engineering environment in a single simulation cockpit.



5G NR Library in PathWave System Design (SystemVue) Key Benefits:

- Model baseband, RF, and antennas in a single tool
- Use trusted algorithm reference IP
- Model RF system architecture
- Perform advanced end-to-end link performance
- Setup over-the-air simulation

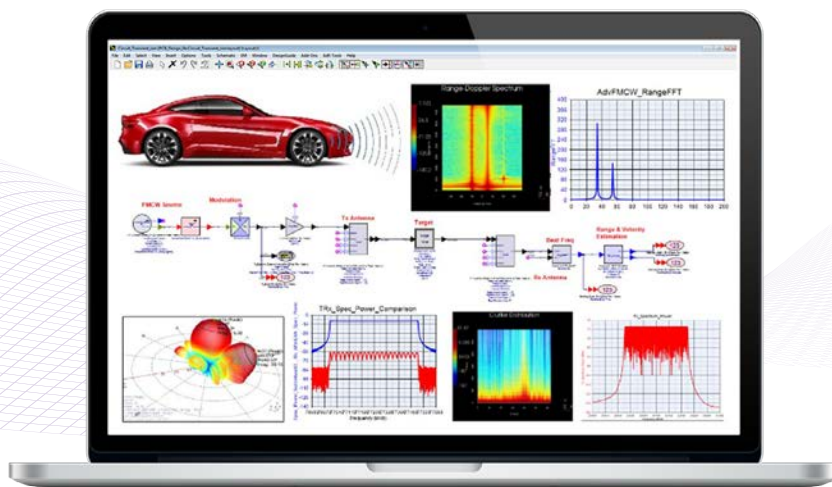
CHALLENGE 2: Automotive radar designers must ensure safety with accurate simulations

Automotive radar is evolving from convenience functions, like adaptive cruise control and safety warning systems, to intelligent detection and collision mitigation systems. Increasingly, automotive developers are adopting higher-frequency radar systems, offering higher performance with greater reliability, and more accurate spatial resolution between different objects, enhancing the vehicle's ability to respond to potential dangers on the road.

With motorist and pedestrian lives at stake, there is little room for design error. Chip designers must prove their devices in a reference system simulation scenario to ensure safety. That scenario must consider detection range with accuracy, as well as mmWave propagation, multi-GHz bandwidths and interference, and RF impairments. Capturing complex moving targets in the presence of clutter is also a must for radar designers. Bringing field scenarios into iterative system simulation can help minimize any technical risks.

SOLUTION: Automotive Radar Library in PathWave System Design (SystemVue)

The **Automotive Radar Library** is used to integrate critical, safety-conscious and complicated scenarios into reliable, leading-edge design of automotive radar. It provides solutions for cost and time constrained projects that enable the design and development of algorithms such as direction of angle (DOA) and phase comparison. The Automotive Radar Library has comprehensive tools for radar waveform generation, signal modulation, antenna modeling, channel simulation and signal processing. Users simply connect different models to establish the unique automotive radar simulation scenarios.



Automotive Radar Library in PathWave System Design (SystemVue) Key Benefits:

- Multi-scatter target parameterized simulation models
- Reference designs for scenario simulation
- Synergistic system simulation tools for RF and baseband
- Frequency- and time-domain simulation
- Co-simulation with PathWave ADS, PathWave Vector Signal Analysis (VSA), and MATLAB



Device Modeling Solutions

The semiconductor industry faces continuing challenges to maximize product performance and yield, decrease time-to-market, and reduce production costs. As device geometries get smaller, the need to use accurate models and to control statistical variations in device processing performance becomes ever more important. Typical circuit operating frequencies continue to advance well into the RF and microwave frequency range. Accurate device models are critical to circuit simulation convergence and accuracy. Circuit designers need models that can accurately predict device behaviors at DC, and in the RF and microwave regions.



CHALLENGE: Modeling thermal effects and complex circuits with GaN technology

The increasing demand for 5G and radar applications are driving the industry toward Gallium Nitride (GaN) technologies, with their superior power, size and efficiency advantages. Circuits are being pushed to higher frequencies as device geometries are becoming smaller with higher chip device counts. Modeling GaN devices is challenging due to the impact of trapping and thermal effects on the device's electrical characteristics. Designers need a software tool to perform the necessary measurements and extraction of GaN devices.

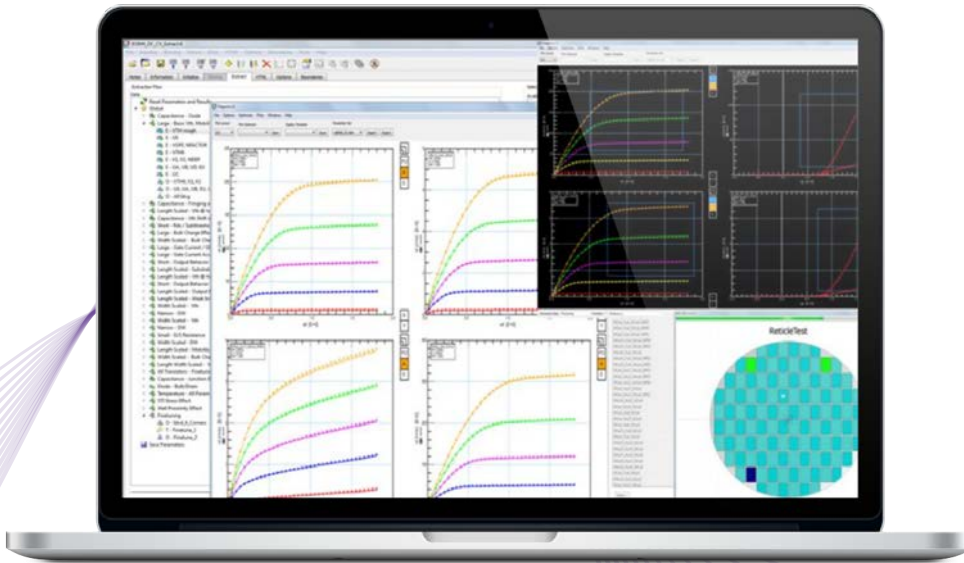
SOLUTION: PathWave Device Modeling (IC-CAP)

PathWave Device Modeling (IC-CAP) is a versatile and user-programmable industry standard for semiconductor device modeling. Users can write custom extraction routines, create user interface dialogs, and automate extraction flows. PathWave Device Modeling (IC-CAP) gives access to cutting edge modeling technology for compound semiconductor devices.



PathWave Device Modeling (IC-CAP) Key Benefits:

- Advanced graphical user interface (GUI)
- PEL and Python programming for data post processing
- Efficient data management
- Wide choice of industry standard simulators
- 13 powerful optimization algorithms



SOLUTION: PathWave Model Builder

PathWave Model Builder is a complete silicon turnkey device modeling software. It integrates device simulation, model parameter extraction, and optimization. PathWave Model Builder supports all popular compact models including the latest BSIM-CMG, BSIM-IMG, and BSIM6 for DC, AC, and RF applications. The open interface enables optimization flow customization, device target definition, and the ability to define GUI operations.



PathWave Model Builder Key Benefits:

- Comprehensive model extraction solution
- Predefined templates for high-voltage device modeling
- Design for manufacturing (DFM) and layout device modeling capabilities
- Optimization of macro variables and model parameters together

SOLUTION: PathWave Model QA

SPICE model validation is a critical step in the device modeling design flow, but difficult to conduct automatically. **PathWave Model QA** is the industry standard SPICE model signoff and acceptance software. Users can easily use it to identify model issues with customizable knowledge-based checking routines. PathWave Model QA performs comparison and documentation automatically, while ensuring design success using advanced process technologies.



PathWave Model QA Key Benefits:

- Integrated sets of rules to ensure accurate SPICE models
- Fully customizable rules and check functions
- Quick measurement QA, model comparison, and corner model QA
- Powerful equation viewer

SOLUTION: PathWave WaferPro

PathWave WaferPro programming test software performs wafer-level measurements of semiconductor devices such as transistors and circuit components. It can be used with a variety of instruments and wafer probes. With the software, users can quickly and easily setup and execute automated wafer-level measurements.



PathWave WaferPro Key Benefits:

- Modern and intuitive user interface
- Automatic temperature and positioning controls
- Extensive library of semiconductor device configurations
- Custom drivers and tests with Python and other programming
- Wafer data mapping viewer

To learn more, go to www.keysight.com/us/en/products/design-software.html

Keysight Services



Test Asset Optimization Services Keysight Test Asset Optimization services capture real-time, actionable utilization and health data to dramatically decrease capital and operating expenses. **PathWave Asset Advisor** identifies the “real” situation of your assets by location, user, firmware, software version and more. It is at the core of a data-driven asset optimization program and significantly improves return on test investment.



Test-as-a-Service The design challenges of wireless standards and regulations are increasingly more complex. **Keysight Test as a Service (TaaS)** helps you face the challenges of increasing test complexity, budget constraints, and limited technical resources. Our quality test labs and experts will help you keep ahead of the latest compliance requirements.



Technology Refresh Services Whether you are migrating to a new technology, extending the life of an existing system, or developing a new program, Keysight has solutions to assist you. **Technology Refresh** offers an easy and cost-effective way to upgrade or trade-in existing assets to obtain the test equipment performance for your new requirements.



Education Services With **eLearning**, you'll gain the basic skills needed to make more accurate, repeatable measurements. Start-Up Assistance complements that skillset with private, customized hands-on instruction specifically designed to help you get your application measurement objectives met.



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