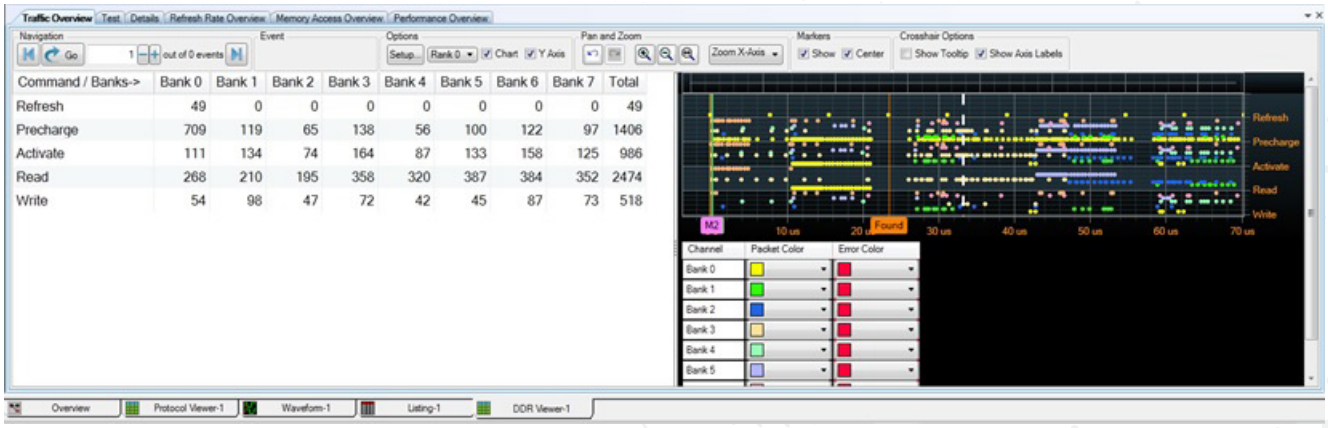
DATA SHEET

# B4661A Memory Analysis Software for Logic Analyzers




KEYSIGHT TECHNOLOGIES

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# Overview

The Keysight B4661A memory analysis software offers a suite of viewers and tools that include the industry's first protocol compliance violation testing capability across speed changes, a condensed traffic overview for rapid navigation to areas of interest in the logic analyzer trace, powerful performance analysis graphics, and DDR and LPDDR decoders. With the B4661A memory analysis software and a Keysight logic analyzer, users can monitor DDR3/4/5 or LPDDR2/3/4/5 systems to debug, improve performance, and validate protocol compliance. Powerful traffic overviews, multiple viewing choices, and real-time compliance violation triggering help identify elusive DDR/LPDDR system violations.

The Keysight B4661A memory analysis software provides four standard software features and seven licensed memory analysis options. GDDR6 analysis (B4661A-7FP/7TP/7NP) will be added in the 6.60 release in January 2020.

Licensed software options

- DDR decoder with physical address trigger tool (B4661A-1NP/1TP/1NP)
- LPDDR decoder with physical address trigger tool for LPDDR/2/3 (B4661A-2NP/2TP/2FP)
- DDR and LPDDR compliance violation analysis toolset (B4661A-3NP/3TP/3FP)
  - Post-process compliance violation analysis
  - Real-time compliance violation analysis
- DDR3/4, LPDDR2/3/4, and ONFi (Open NAND Flash interface) analysis (B4661A-4NP/4TP/4FP)
- DDR5 Analysis and Compliance SW (B4661A-5NP/5TP/5FP)
- LPDDR5 Analysis and Compliance SW (B4661A-6NP/6TP/6FP)
- GDDR6 analysis (B4661A-7FP/7TP/7NP)

Standard software features

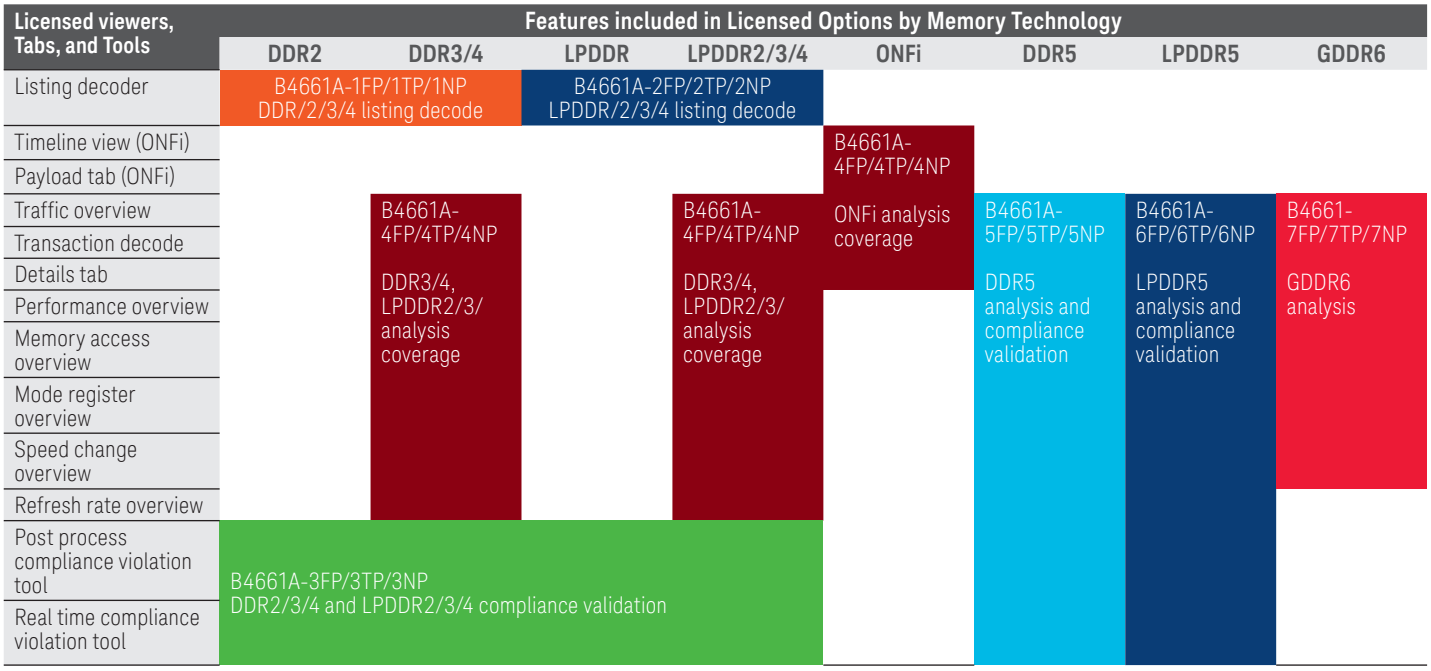
- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator


Use the optional compliance violation analysis and performance tools to further debug, validate, and optimize your memory system. (See pages 5 to 28)
Start with Keysight's standard DDR/LPDDR tools to help setup your measurement (see pages 32 to 38).
– Standard configuration files for Keysight and FuturePlus interposers are provided.
– If a standard configuration is not available for your probing solution, the DDR/LPDDR configuration creator enables you to quickly create a configuration file relative to your system's layout.
– Setup assistant and eye scan help you get sampling positions, thresholds, and triggering adjusted for a good measurement.
– Eye scan also helps you identify multiple signal integrity and execution issues before you even take your first trace capture with your logic analyzer module.

# Licensed Views and Tools

Use the licensed optional viewers and tools for analysis, transaction decode, performance, and compliance violation insight to further debug, validate, and optimize your memory system. Monitor memory activity and follow the memory signal flow like a device on the memory bus.

Chart of licensed viewers, tabs, and tools by recommended options for memory technologies.



# Traffic Overview

## Command graphing

Using traffic overview, each command on the bus is a row in the table. Columns vary depending on the viewing option chosen. Users choose from the following viewing options:

- View all ranks – in this mode, the table columns are “All ranks,” “Rank 0,” Rank 1,” etc. The chart shows a different color dot on a different line for each rank.
- View a single rank – The table columns are “All banks,” “Bank 0,” etc. (For DDR4, the columns are “All BG/BA”, then all combinations of BG and BA.) The chart shows one line of dots. A choice for which bank to view in the chart is enabled.
- All banks – The chart shows a dot for every command on the rank, regardless of bank. All dots are the same color.
- A single bank – The chart shows a dot for commands that apply only to the selected bank.
- If the user has a multi-rank system and wants to see charts of each rank simultaneously, then they can use multiple applications of the tool.

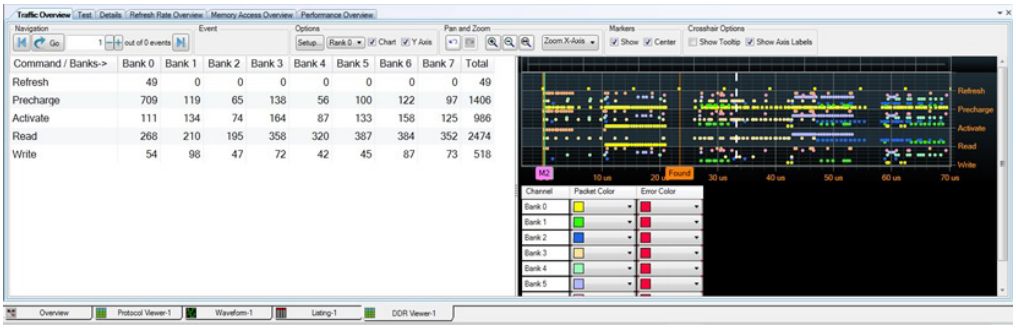
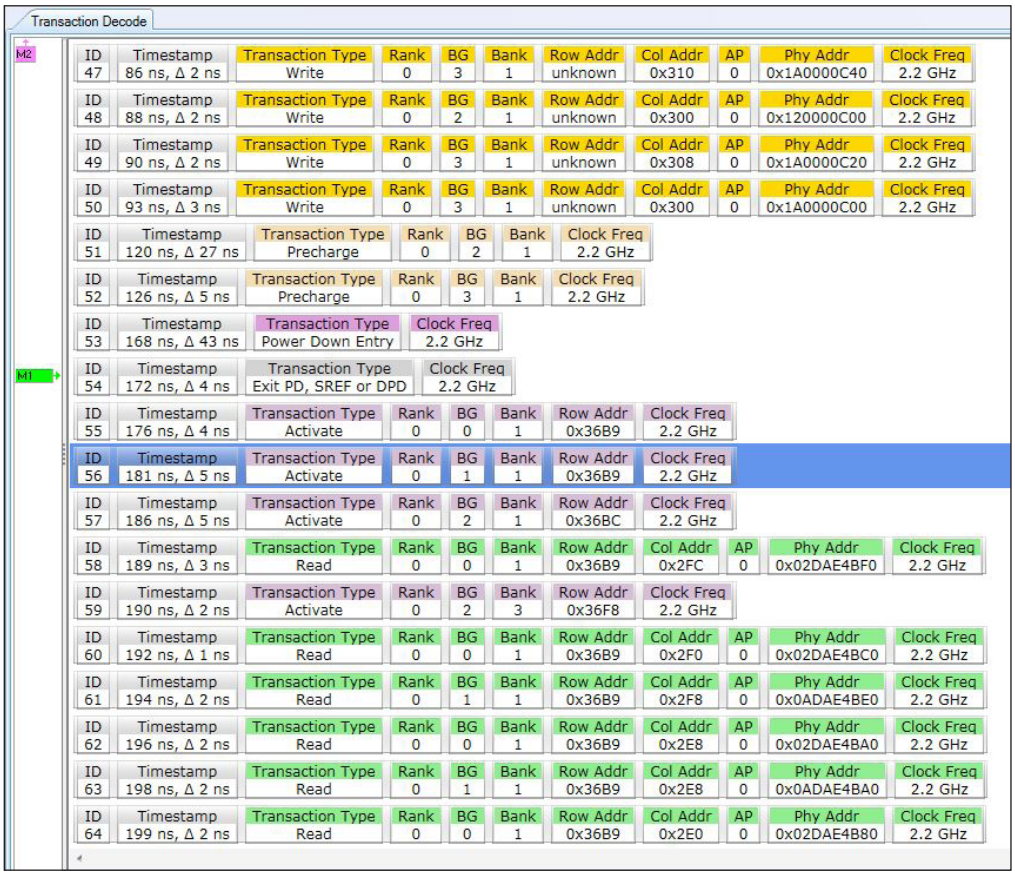



Figure 1. Traffic overview example: Graphing command activity by commands and banks across the captured trace from the Keysight logic analyzer.

The traffic overview containing transaction decode, summary calculations, meta-data, and graphing provides a condensed and insightful overview of system activity and enables powerful navigation to areas of interest.

# Transaction Decode




| ID | Timestamp | Transaction Type | Rank | BG | Bank | Row Addr | Col Addr | AP | Phy Addr | Clock Freq |
|---|---|---|---|---|---|---|---|---|---|---|
| 47 | 86 ns, Δ 2 ns | Write | 0 | 3 | 1 | unknown | 0x310 | 0 | 0x1A0000C40 | 2.2 GHz |
| 48 | 88 ns, Δ 2 ns | Write | 0 | 2 | 1 | unknown | 0x300 | 0 | 0x120000C00 | 2.2 GHz |
| 49 | 90 ns, Δ 2 ns | Write | 0 | 3 | 1 | unknown | 0x308 | 0 | 0x1A0000C20 | 2.2 GHz |
| 50 | 93 ns, Δ 3 ns | Write | 0 | 3 | 1 | unknown | 0x300 | 0 | 0x1A0000C00 | 2.2 GHz |
| 51 | 120 ns, Δ 27 ns | Precharge | 0 | 2 | 1 | | | | | 2.2 GHz |
| 52 | 126 ns, Δ 5 ns | Precharge | 0 | 3 | 1 | | | | | 2.2 GHz |
| 53 | 168 ns, Δ 43 ns | Power Down Entry | | | | | | | | 2.2 GHz |
| 54 | 172 ns, Δ 4 ns | Exit PD, SREF or DPD | | | | | | | | 2.2 GHz |
| 55 | 176 ns, Δ 4 ns | Activate | 0 | 0 | 1 | 0x36B9 | | | | 2.2 GHz |
| 56 | 181 ns, Δ 5 ns | Activate | 0 | 1 | 1 | 0x36B9 | | | | 2.2 GHz |
| 57 | 186 ns, Δ 5 ns | Activate | 0 | 2 | 1 | 0x36BC | | | | 2.2 GHz |
| 58 | 189 ns, Δ 3 ns | Read | 0 | 0 | 1 | 0x36B9 | 0x2FC | 0 | 0x02DAE4BF0 | 2.2 GHz |
| 59 | 190 ns, Δ 2 ns | Activate | 0 | 2 | 3 | 0x36F8 | | | | 2.2 GHz |
| 60 | 192 ns, Δ 1 ns | Read | 0 | 0 | 1 | 0x36B9 | 0x2F0 | 0 | 0x02DAE4BC0 | 2.2 GHz |
| 61 | 194 ns, Δ 2 ns | Read | 0 | 1 | 1 | 0x36B9 | 0x2F8 | 0 | 0x0ADAE4BE0 | 2.2 GHz |
| 62 | 196 ns, Δ 2 ns | Read | 0 | 0 | 1 | 0x36B9 | 0x2E8 | 0 | 0x02DAE4BA0 | 2.2 GHz |
| 63 | 198 ns, Δ 2 ns | Read | 0 | 1 | 1 | 0x36B9 | 0x2E8 | 0 | 0x0ADAE4BA0 | 2.2 GHz |
| 64 | 199 ns, Δ 2 ns | Read | 0 | 0 | 1 | 0x36B9 | 0x2E0 | 0 | 0x02DAE4B80 | 2.2 GHz |

Figure 2. Transaction decode provides a high-level view of the memory protocol transactions.

# Performance Overview

## Calculate and graph MByte data rates and % utilization

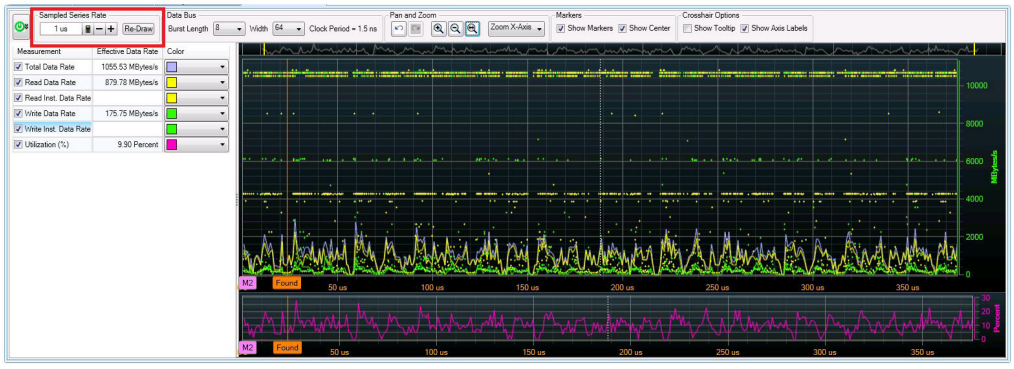



Figure 3. Customize performance views by changing sample rate and performance measurement selections.

The Performance Overview provides graphical and summary calculations of Read, Write, and Total MByte data rates along with a calculation and graph of the percentage of bus utilization. Users can choose to view the Read or Write Data rates as instantaneous, where each Read or Write command is represented with a dot.

# Address Access Mapping

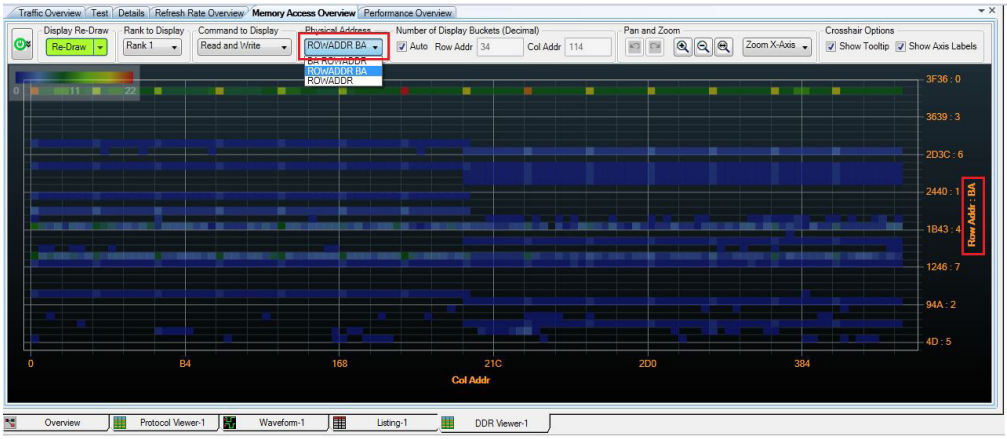



Figure 4. Address access heat map enables an overview of the number of accesses at specific row and col addresses.

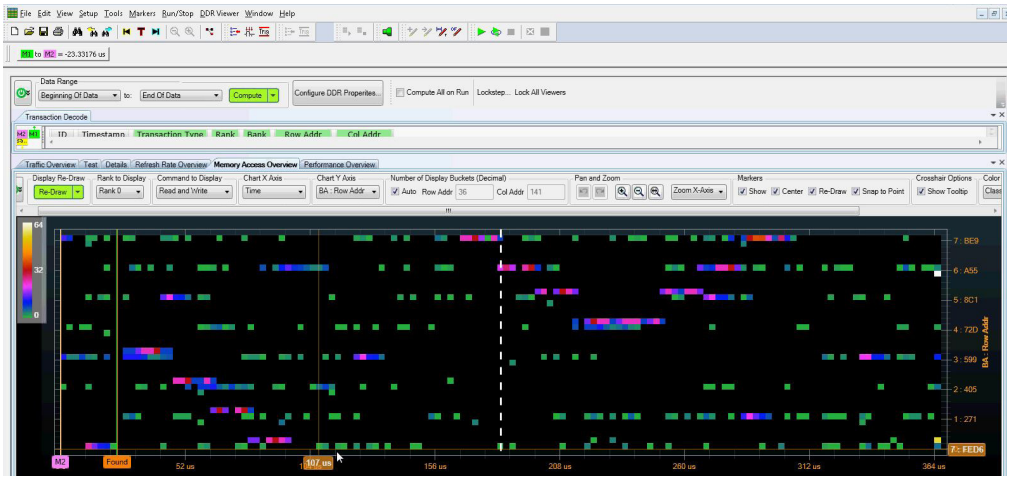



Figure 5. Users may also select row address and time as the axis on the address access heat map.

# Refresh Rate Overview

DDR/LPDDR memory is volatile. The charge on the memory cells (capacitors) needs to be “refreshed” to ensure memory values are retained. For DDR and LPDDR memory, there are two ways to refresh

- Issue the refresh command.
- Issue a self-refresh command and put the memory into self-refresh mode for some length of time.

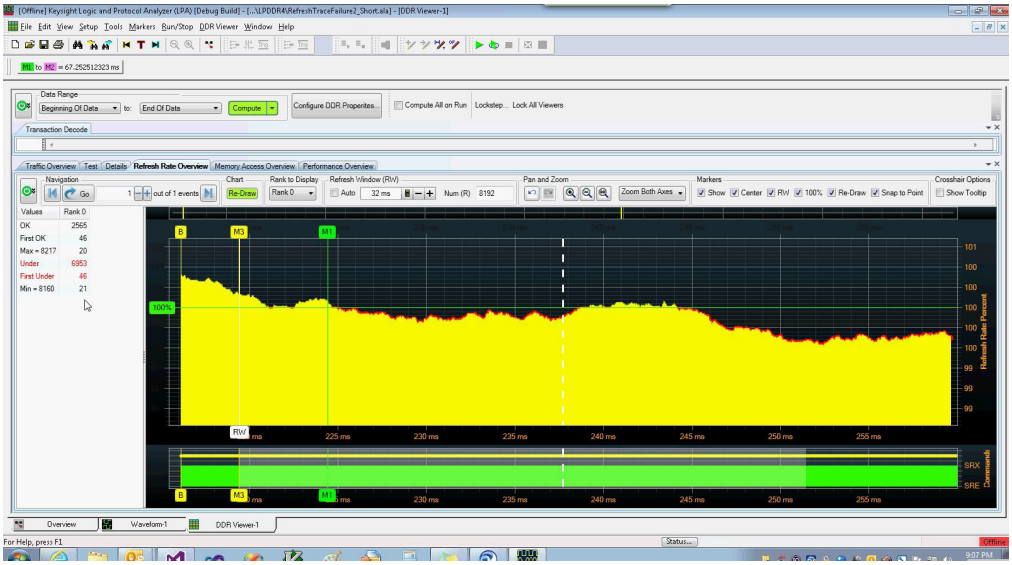


Figure 6. Refresh rate charts of LPDDR4 trace activity and quick pass/fail indication.

The refresh rate overview provides insight into refresh performance. It graphs refresh rate information for each sampled RW (refresh window) time window. By default, new refresh window samples are taken whenever there is a refresh event: refresh commands or entering/exiting self-refresh mode.

The X axis of this chart is time. The Y coordinate is the percent scale of expected refresh commands and self-refresh time found in the time window. The horizontal green line represents 100% for quick pass/fail indication. Red dots indicate areas that are under 100%.

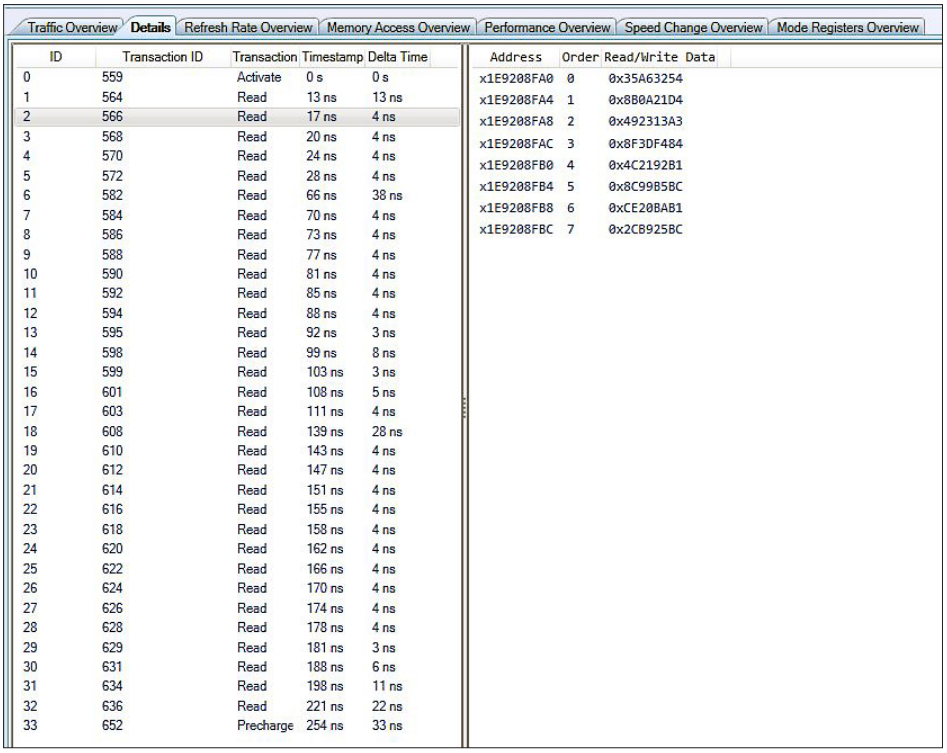
Users can set the refresh window time (default 32 ms), the number (R) of refresh commands expected in the refresh window time, and the rank to display.

The highlighted box in the lower chart shows the refresh window time span for the sample at the “RW” marker point. The highlight box is red when under 100% and white when >= 100%.

# Details Tab

For LPDDR2/3/4/5, DDR3/4/5, and GDDR6, this tab displays the details of a selected memory transaction and all other transactions in the same sequence or 'open/closed page'. 'Pages' open with Activate commands, all Reads or Writes associated with the same Rank, Bank Group, Bank, and Row Address are part of the 'open page'. Pages close with an associated Precharge. When either a Read or Write transaction is selected, the Data associated with the selected Read or Write is also displayed with the associated address.

For ONFi, this tab displays the details of an ONFi transaction selected in the upper pane. You can also visualize an ONFi operation as a set of logically grouped commands in a sequence in the details tab.




| ID | Transaction ID | Transaction | Timestamp | Delta Time |
|---|---|---|---|---|
| 0 | 559 | Activate | 0 s | 0 s |
| 1 | 564 | Read | 13 ns | 13 ns |
| 2 | 566 | Read | 17 ns | 4 ns |
| 3 | 568 | Read | 20 ns | 4 ns |
| 4 | 570 | Read | 24 ns | 4 ns |
| 5 | 572 | Read | 28 ns | 4 ns |
| 6 | 582 | Read | 66 ns | 38 ns |
| 7 | 584 | Read | 70 ns | 4 ns |
| 8 | 586 | Read | 73 ns | 4 ns |
| 9 | 588 | Read | 77 ns | 4 ns |
| 10 | 590 | Read | 81 ns | 4 ns |
| 11 | 592 | Read | 85 ns | 4 ns |
| 12 | 594 | Read | 88 ns | 4 ns |
| 13 | 595 | Read | 92 ns | 3 ns |
| 14 | 598 | Read | 99 ns | 8 ns |
| 15 | 599 | Read | 103 ns | 3 ns |
| 16 | 601 | Read | 108 ns | 5 ns |
| 17 | 603 | Read | 111 ns | 4 ns |
| 18 | 608 | Read | 139 ns | 28 ns |
| 19 | 610 | Read | 143 ns | 4 ns |
| 20 | 612 | Read | 147 ns | 4 ns |
| 21 | 614 | Read | 151 ns | 4 ns |
| 22 | 616 | Read | 155 ns | 4 ns |
| 23 | 618 | Read | 158 ns | 4 ns |
| 24 | 620 | Read | 162 ns | 4 ns |
| 25 | 622 | Read | 166 ns | 4 ns |
| 26 | 624 | Read | 170 ns | 4 ns |
| 27 | 626 | Read | 174 ns | 4 ns |
| 28 | 628 | Read | 178 ns | 4 ns |
| 29 | 629 | Read | 181 ns | 3 ns |
| 30 | 631 | Read | 188 ns | 6 ns |
| 31 | 634 | Read | 198 ns | 11 ns |
| 32 | 636 | Read | 221 ns | 22 ns |
| 33 | 652 | Precharge | 254 ns | 33 ns |

| Address | Order | Read/Write Data |
|---|---|---|
| x1E9208FA0 | 0 | 0x35A63254 |
| x1E9208FA4 | 1 | 0x8B0A21D4 |
| x1E9208FA8 | 2 | 0x492313A3 |
| x1E9208FAC | 3 | 0x8F3DF484 |
| x1E9208FB0 | 4 | 0x4C2192B1 |
| x1E9208FB4 | 5 | 0x8C99B5BC |
| x1E9208FB8 | 6 | 0xCE20BAB1 |
| x1E9208FBC | 7 | 0x2CB925BC |

Figure 7. The Details tab provides Page associations and associated Data for any highlighted Read or Write transaction.

# Speed Change Overview

Speed Change Overview provides a statistical as well as a graphical representation for an SDRAM's clock frequencies and frequency changes over a period of time.

- Higher pulses = higher frequency
- Duration of pulse = time at specific frequency

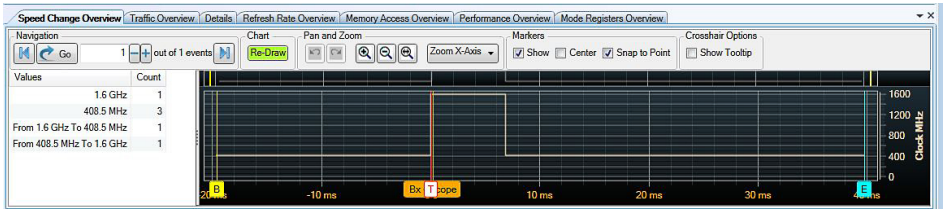



Figure 8. Speed changes on an LPDDR4 system.

# Mode Registers Overview

## Analyzing mode registersvalues

The Mode Registers Overview tab of the DDR/LPDDR Memory Analysis window provides you the following data from the computed memory transactions:

- A count of the Mode Register commands found for each of the mode registers of your SDRAM. For a multi-rank SDRAM, these counts are displayed for the mode registers of each of the ranks.
- A snapshot of the SDRAM's mode registers' values at a specific time.
- A comparison of the state of mode registers at different points in time.

or across ranks at a specific point in time. You can use the data displayed in this tab to get an insight into the state of the various operating parameters of the SDRAM that have been configured using various mode registers of the SDRAM. The comparison of the mode register values can help you understand and debug the SDRAM's behavior due to mode register value changes.

The following memory commands that are issued to set or modify mode registers of an SDRAM are included in the Mode Register Overview tab's data:

- Mode Register Set command
- Mode Register Write command

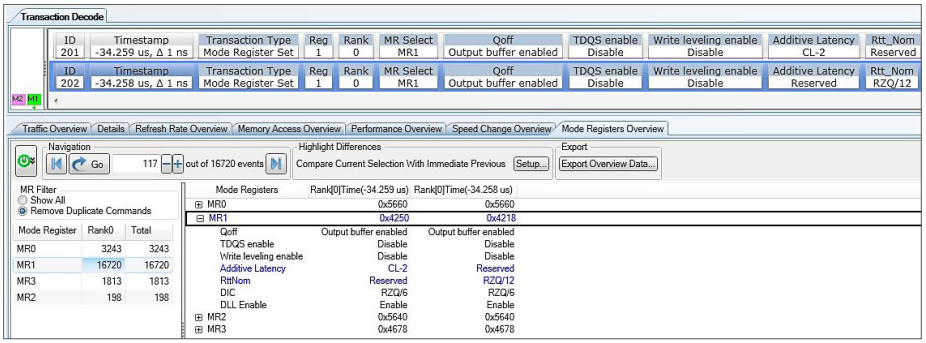



Figure 9. Mode Register Overview.

# GDDR6 Analysis (B4661A-7FP/7TP/7NP)

Using the B4661 memory analysis licensed software for GDDR6 analysis, navigation to problem areas is simplified with a powerful traffic overview that presents the GDDR6 traffic from the logic analyzer trace capture at the protocol level with user-selected filtering.

Licensed option B4661A-7FP/7TP/7NP consists of a GDDR6 analysis viewer with multiple tabs/views.

Key features (views and tools are described in more detail with screen shot examples under sections specific to each view or toolŁ)

- Traffic overview
- Graphs commands across the trace timeline
- Transaction decode
- Supports decoding of bank organization modes
- Decodes multipurpose (MPC) commands
- Details tab to see the data associated with each read or write transaction
- Performance overview
- Calculates and graphs data rates and % bus utilization
- Memory access overview
- Maps address accesses
- By row and Col ADDR
- By row ADDR and time
- Mode register overview
- Speed change overview

# LPDDR5 Analysis and Compliance Validation (B4661A-6FP/6TP/6NP)

Achieve greater insight faster using the B4661 memory analysis and compliance validation licensed software for LPDDR5 memory. LPDDR testing, protocol compliance and debug work has become more complex and time consuming over the years as data rates increase and the memory architectures become more complex. Using the LPDDR5 analysis and protocol compliance validation, navigation to problem areas is simplified with a powerful traffic overview that presents the LPDDR5 traffic from the logic analyzer trace capture at the protocol level with user-selected filtering.

Licensed option B4661A-6FP/6TP/6NP consists of a LPDDR5 analysis viewer with multiple tabs/views and two LPDDR5 protocol compliance tools, a Real-time DDR5 protocol compliance tool and a Post-process LPDDR5 protocol compliance tool.

## LPDDR5 analysis

Key features (these views and tools are described in more detail with screen shot examples under sections specific to each view or tool.

- Traffic overview
  - Graphs commands across the trace timeline
- Transaction decode
  - Supports decoding of bank organization modes
  - Decodes multipurpose (MPC) commands
  - Self-Refresh entry/exit
- Details tab to see the data associated with each read or write transaction
- Performance overview
  - Calculates and graphs MByte data rates and % bus utilization
- Memory access overview
  - Maps Address accesses
    - By row and Col ADDR
    - By row ADDR and time
- Refresh rate overview
- Speed Change overview
- Mode Register overview

## LPDDR5 protocol compliance tools

- LPDDR5 Real-time compliance violation analysis
- LPDDR5 Post-process violation analysis

Key features of both the post-process and real-time compliance violation tools:

- Test compliance violations across speed changes using the post-process compliance violation tool.
- Identify LPDDR5 state machine, protocol compliance, and protocol level bus cycle timing violations using either post-process or real-time tools.
- Save time with automated real-time LPDDR5 protocol compliance measurements and trace captures using the real-time compliance violation analysis tool.
- Edit parameters of the LPDDR5 standard preset tests easily using the enhanced parameter editing interface for both post-process and real-time tools.

## Real-time LPDDR5 protocol compliance analysis

The automated real-time compliance analysis tool detects and captures state machine, protocol compliance, and protocol level bus cycle timing violations for LPDDR5. Real-time violation detection is an important advancement in DDR memory debug and valida¬tion. Monitoring your LPDDR5 bus real-time means the Keysight logic analyzer will continuously monitor the bus for the selected test and trigger if it occurs within the specified time.

## LPDDR5 Real-time testing enables

Monitoring for compliance violations while running specific routines on the system under test. Unique feature of real-time compliance tool allows custom regression test suites to be created from a valid logic analyzer trigger for any valid Keysight logic analyzer configuration compatible with the B4661A.

The real-time compliance violation analysis tool cycles through preset or user-edited parameters for a selectable time limit on each parameter to capture logic analyzer traces of the DDR5 bus, triggering on the violation. The tool allows the user to save multiple traces of violations and produces a summary report when complete.

## Post-process LPDDR5 protocol compliance violation analysis tool

The post-process compliance violation analysis tool automates state machine, protocol compliance, and protocol level bus cycle timing violation detection across Keysight logic analyzer traces.HTML reports of test results show margin details for both passing and failing tests. Use the post-process compliance application tool to:

- Spot check logic analyzer traces for violations.
- Check logic analyzer trace captures leading up to system crashes for possible violations before the crash.

## Post-process testing enables

- Compliance violation testing across speed changes.
- “Click to” and “mark violation” features to quickly navigate from the compliance tool to violations in the traffic overview graph, waveform, or listing window.
- Margin information on each parameter to understand the range relative to the specification.

# DDR5 Analysis and Compliance Validation (B4661A-5FP/5TP/5NP)

Achieve greater insight faster using the B4661 memory analysis and compliance validation licensed software for DDR5 memory. DDR testing, protocol compliance and debug work has become more complex and time consuming over the years as data rates increase and the memory architectures become more complex. Using the DDR5 analysis and protocol compliance SW, navigation to problem areas is simplified with a powerful traffic overview that presents the DDR5 traffic from the logic analyzer trace capture at the protocol level with user-selected filtering.

Licensed option B4661A-5FP/5TP/5NP consists of a DDR5 analysis viewer with multiple tabs/views and two DDR5 protocol compliance tools, a Real-time DDR5 protocol compliance tool and a Post-process DDR5 protocol compliance tool.

## DDR5 analysis

Key features (these views and tools are described in more detail with screen shot images under sections specific to each view or tool.

- Traffic overview
  - Graphs commands across the trace timeline
- Transaction decode
  - Supports decoding of low power data transfers
  - Decodes multipurpose (MPC) commands
  - Self-Refresh entry/exit
- Details tab to see the data associated with each read or write transaction
- Performance overview
  - Calculates and graphs MByte data rates and % bus utilization
- Memory access overview
  - Maps Address accesses
    - By row and Col ADDR
    - By row ADDR and time
- Refresh rate overview
- Speed Change overview
- Mode Register Overview

## DDR5 protocol compliance tools

- DDR5 Real-time protocol compliance violation analysis
- DDR5 Post-process protocol compliance violation analysis

Key features of both the post-process and real-time compliance violation tools:

- Test compliance violations across speed changes using the post-process compliance violation tool.
- Identify DDR5 state machine, protocol compliance, and protocol level bus cycle timing violations using either post-process or real-time tools.
- Save time with automated real-time DDR5 protocol compliance measurements and trace captures using the real-time compliance violation analysis tool.
- Edit parameters of the DDR5 standard preset tests easily using the enhanced parameter editing interface for both post-process and real-time tools.

## Real-time DDR5 compliance analysis

The automated real-time compliance analysis tool detects and captures state machine, protocol compliance, and protocol level bus cycle timing violations for DDR5. Real-time violation detection is an important advancement in DDR memory debug and validation. Monitoring your DDR5 bus real-time means the Keysight logic analyzer will continuously monitor the bus for the selected test and trigger if it occurs within the specified time.

## Real-time testing enables

Monitoring for compliance violations while running specific routines on the system under test. Unique feature of real-time compliance tool allows custom regression test suites to be created from a valid logic analyzer trigger for any valid Keysight logic analyzer configura¬tion compatible with the B4661A.

The real-time compliance violation analysis tool cycles through preset or user-edited parameters for a selectable time limit on each parameter to capture logic analyzer traces of the DDR5 bus, triggering on the violation. The tool allows the user to save multiple traces of violations and produces a summary report when complete.

## Post-process DDR5 compliance violation analysis tool

The post-process compliance violation analysis tool automates state machine, protocol com¬pliance, and protocol level bus cycle timing violation detection across Keysight logic analyzer traces.HTML reports of test results show margin details for both passing and failing tests. Use the post-process compliance application tool to:

- Spot check logic analyzer traces for violations.
- Check logic analyzer trace captures leading up to system crashes for possible violations before the crash.

## Post-process testing enables

- Compliance violation testing across speed changes.
- “Click to” and “mark violation” features to quickly navigate from the compliance tool to violations in the traffic overview graph, waveform, or listing window.
- Margin information on each parameter to understand the range relative to the specification.

# DDR3/4, LPDDR2/3/4, Analysis and ONFi Analysis (B4661A-4FP/4TP/4NP)

Licensed option B4661A-4FP/4TP/4NP consists of two different analysis viewers. One viewer covers DDR3/4 and LPDDR2/3/4 analysis and the second viewer provides ONFi analysis.

## DDR3/4 and LPDDR2/3/4 Analysis Viewer

Key features

- Traffic overview
  - Command graphing
- Transaction decode
- Performance overview
  - Calculate and graph MByte data rates and % bus utilization
- Memory access overview, address access mapping
  - By row and Col ADDR
  - By row ADDR and time
- Refresh rate overview
- Speed Change Overview
- Mode register overview

## ONfi (Open NAND Flash interface) Analysis Viewer

Key features

- Timeline View
- Payload tab
- Details tab
- Customizable features to support Toggle mode and proprietary NAND protocols

# ONFi Analysis Viewer

Enhanced ONFi (open NAND flash interface) analysis is included in the B4661A Memory analysis SW, licensed option -4NP/TP/FP.

- Follow ONFi traffic flow using “Transaction Decode” and “Traffic Overview” views.
- Navigate quickly across multiple ONFi targets using the condensed ONFi analysis “Timeline” view.
- Save time by visualizing an ONFi operation as a set of logically associated commands in a sequence, using the “Details” view of the ONFi transactions.

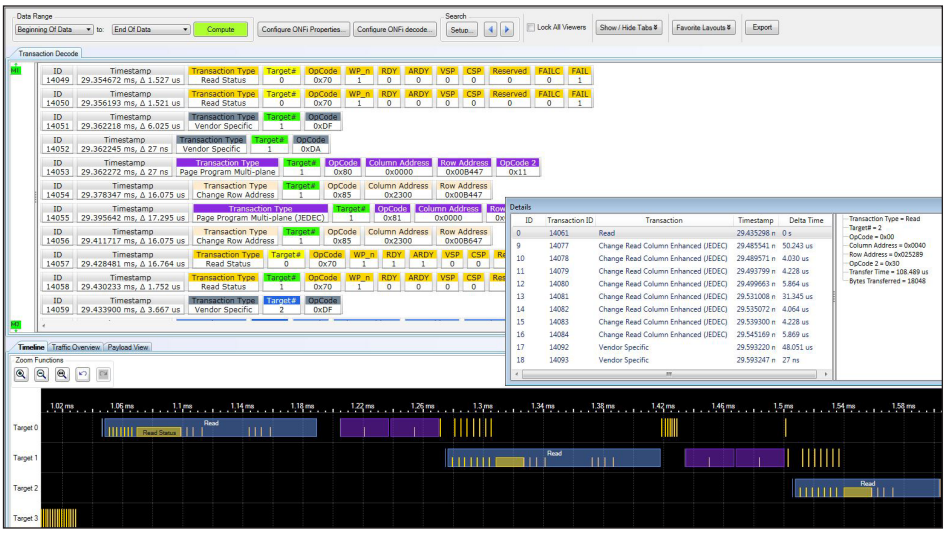


Figure 10. ONFi Transaction Decoder, Details, and Timeline views increase insight into ONFi traffic.

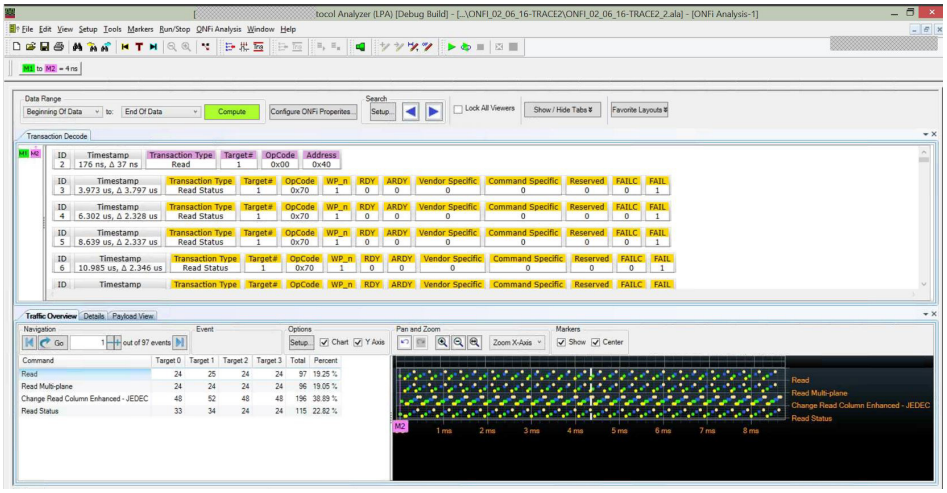


Figure 11. ONFi Traffic Overview with Transaction Decoder provide statistical information and a graphical overview of ONFi transactions over time to allow rapid navigation through the transactions.

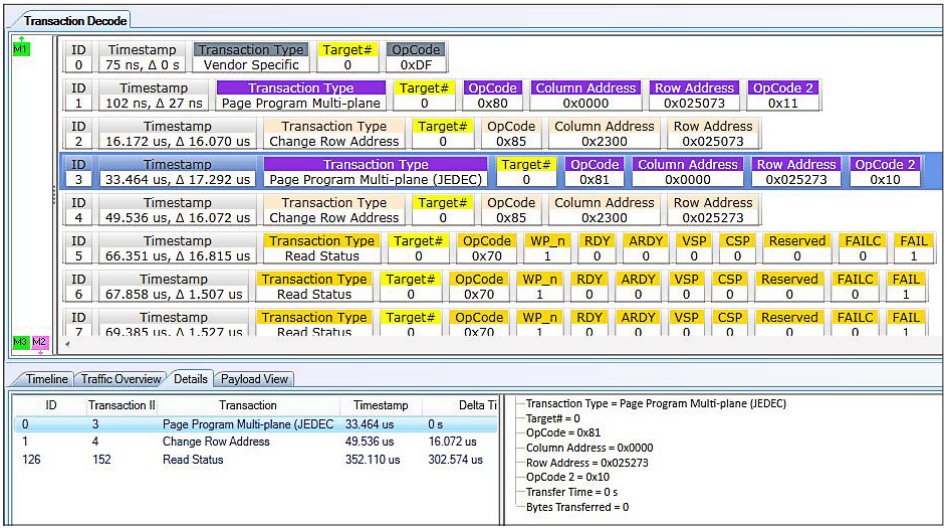



Figure 12. Save time by visualizing an ONFi operation as a set of logically associated commands inclueing the transation times and delta times.

NAND Memory Controllers often use commands and protocols that are not part of the ONFi Standard.

Proprietary intellectual property can be involved with controlling NAND memory. The ONFi analysis viewer includes the ability for a user to define custom opcodes and sequence associations using xml files. Characteristics of the customization feature include:

- Single line xml for single opcode sequences.
- Longer sequences programmable using simple extensible syntax.
- Support for a wide variety of CMD/ADDR/DATA combinations.
- Customizable Decode text and color.

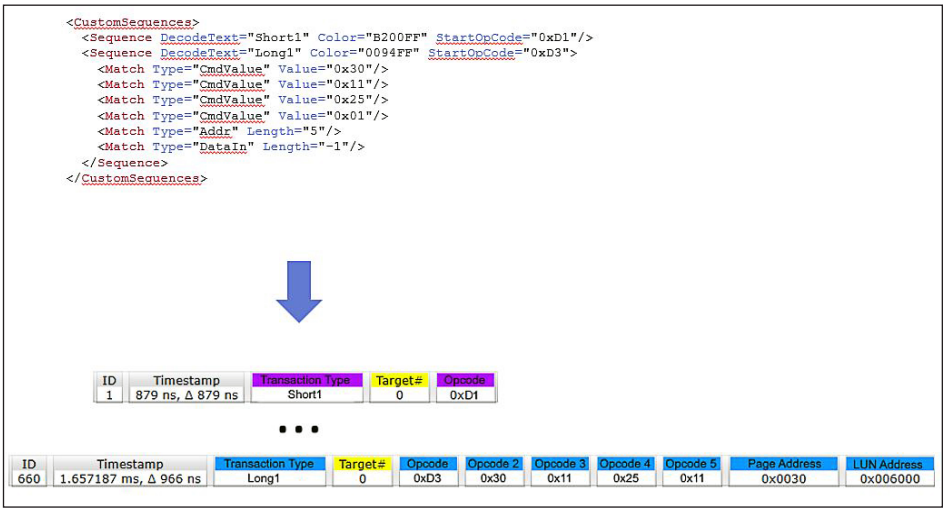



Figure 13. Define custom opcodes and sequence associations.

# DDR and LPDDR Compliance Violation Analysis (B4661A-3FP/3TP/3NP)

The DDR and LPDDR compliance violation analysis toolset provides two tools under one license. Both compliance tools cover DDR, DDR2, DDR3, DDR4, LPDDR, LPDDR2, LPDDR3, and LPDDR4. The two tools are:

- Real-time compliance violation analysis
- Post-process violation analysis

**Keysight often enhances compliance SW parameters. For the latest list of parameters for each technology, download the latest Logic analyzer and B4661A SW.**

Key features of both the post-process and real-time compliance violation tools:

- Test compliance violations across speed changes using the post-process compliance violation tool.
- Identify DDR/2/3/4 or LPDDR/2/3/4 state machine, protocol compliance, and protocol level bus cycle timing violations using either post-process or real-time tools.
- Save time with automated real-time DDR2/3/4 or LPDDR2/3/4 protocol compliance measurements and trace captures using the real-time compliance violation analysis tool.
- Edit parameters of the DDR/LPDDR standard preset tests easily using the enhanced parameter editing interface for both post-process and real-time tools.

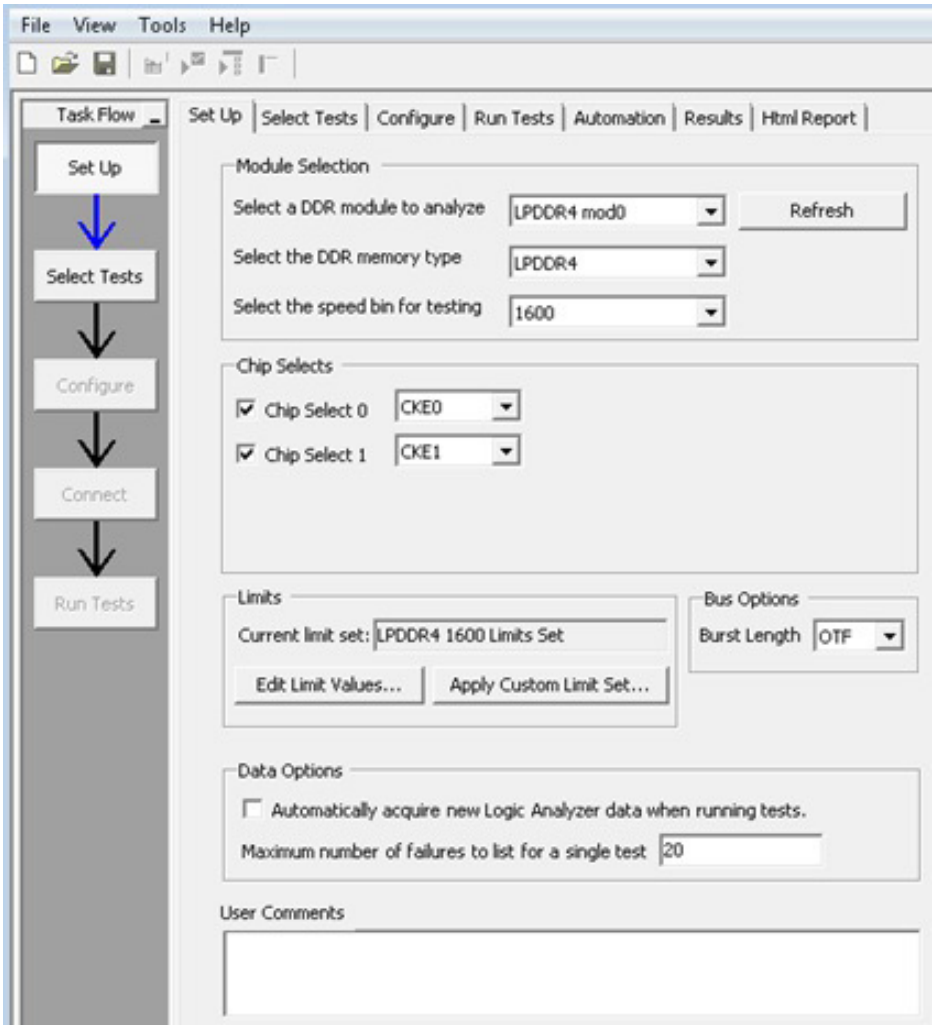



Figure 14. Both the real-time and post-process compliance tools provide user interfaces with pull-down selections to make setup easy.

Post-process and real-time compliance tools both contain dialogs with descriptions of the parameter values for ease of editing.

## Real-time compliance analysis

The automated real-time compliance analysis tool detects and captures state machine, protocol compliance, and protocol level bus cycle timing violations for DDR3/4 or LPDDR2/3/4. Real-time violation detection is an important advancement in DDR memory debug and validation. Monitoring your DDR bus real-time means the Keysight logic analyzer will continuously monitor the bus for the selected test and trigger if it occurs within the specified time frame. Beyond monitoring your DDR3/4 or LPDDR2/3/4 system real-time for elusive violations, designers can also monitor other digital system continuously for elusive, intermittent violations in protocol compliance or bus level timing.

## Real-time testing enables

- Monitoring for compliance violations while running specific routines on the system under test.
- Unique feature of real-time compliance tool allows custom regression test suites to be created from a valid logic analyzer trigger for any valid Keysight logic analyzer configuration compatible with the B4661A.

The real-time compliance violation analysis tool cycles through preset or user-edited parameters for a selectable time limit on each parameter to capture logic analyzer traces of the complete ADD/CMD/DATA capture of the DDR/LPDDR bus triggering on the violation. The tool allows the user to save multiple traces of violations and produces a summary report when complete.

# Real-Time Violations

| **State machine violations common to DDR, DDR2, DDR3, DDR4 and LPDDR, LPDDR2, LPDDR3, LPDDR4** | |
|---|---|
| READ or WRITE to an inactive row | |
| REFRESH to an active bank | |
| ACTIVATE to an active bank | |
| **Real-time violations** | |
| **Compliance parameter** | **Real-time compliance tests** |
| **Parameters common to DDR, DDR2, DDR3, and LPDDR** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRP | PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tDRW | READ to WRITE must be >= tDRW |
| tDWP | WRITE to PRECHARGE must be >= tDWP |
| tCCD | WRITE to WRITE, READ to READ must be >= tCCD |
| tRFC | REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC |
| tRRD | ACTIVATE to ACTIVATE (different banks) must be >= tRRD |
| tRC | ACTIVATE to ACTIVATE (same bank) must be >= tRC |
| tREFI | REFRESH to REFRESH <= tREFI*9 |
| tMRD | MRS (Mode Register Set) to MRS must be >= tMRD |
| **Additional DDR3 compliance parameters** | |
| tZQoper | Long cal (normal operation) to valid command must be >= tZQoper |
| tZQCS | Short calibration (normal operation) to any valid command must be > tZQCS |
| tMOD | MRS (MODE Register Set) to valid command must be >= tMOD |
| tREFPDEN | REFRESH to power down entry >= tREFPDEN |
| tRDPDEN | READ to power down entry >= tRDPDEN |
| tWRPDEN | WRITE to power down entry >= tWRPDEN |
| tXPR | Exit RESET from CKE high to valid command >= tXPR |
| tXSDLL | Self refresh exit to valid command with DLL must be >= tXSDLL |

# Real-Time Violations (Continued)

| Compliance parameter | Real-time compliance tests |
|---|---|
| **Additional DDR4 compliance parameters** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRP | PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tDRW | READ to WRITE must be >= tDRW |
| tDWP | WRITE to PRECHARGE must be >= tDWP |
| tDWR | WRITE to READ must be > tDWR |
| tCCD_L | WRITE to WRITE, same bank group must be >= tCCD_L |
| tRFC | REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC |
| tRRD_L | ACTIVATE to ACTIVATE (same bank group) must be >= tRRD_L |
| tRC | ACTIVATE to ACTIVATE (same bank) must be >= tRC |
| tREFI | REFRESH to REFRESH <= tREFI*9 |
| tZQoper | Long cal (normal operation) to valid command must be >= tZQoper |
| tZQCS | Short calibration (normal operation) to any valid command must be > tZQCS |
| tMRD | MRS (MODE Register Set) to MRS must be >= tMRD |
| tMOD | MRS (MODE Register Set) to valid command must be >= tMOD |
| tREFPDEN | REFRESH to power down entry >= tREFPDEN |
| tRDPDEN | READ to power down entry >= tRDPDEN |
| tWRPDEN | WRITE to power down entry >= tWRPDEN |
| tXPR | Exit RESET from CKE high to valid command >= tXPR |
| tXSDLL | Self refresh exit to valid command with DLL must be >= tXSDLL |
| tCKE | Duration of CKE high / low >= tCKE |
| **Additional LPDDR2/3 compliance parameters** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tDRW | READ to WRITE must be >= tDRW |
| tDWP | WRITE to PRECHARGE must be >= tDWP |
| tDWR | WRITE to READ must be > tDWR |
| tCCD | WRITE to WRITE, must be >= tCCD |
| tRRD | ACTIVATE to ACTIVATE (different banks) must be >= tRRD |
| tZQCL | Long calibration command to any valid command (or CKE low) must be > tZQCL |
| tZQCS | Short calibration command to any valid command (or CKE low) must be > tZQCS |
| tZQINIT | Init calibration command to any valid command (or CKE low) must be > tZQINIT |
| tZQRESET | Reset calibration command to any valid command (or CKE low) must be > tZQRESET |
| tMRW | MRW command to any valid command (or CKE low) must be > tMRW |
| tMRR | MRR command to any valid command (or CKE low) must be > tMRR |
| tRFCab | REFRESH (all banks) to Active or Refresh must be > tRFCab |
| tRFCpb | REFRESH (per bank) to Activate (same bank) or REFRESH must be > tRFCpb |
| tRPab | PRECHARGE (all banks) to ACTIVE (any bank) must be >= tRPab |
| tRPpb | PRECHARGE (per bank) to ACTIVE (same bank) must be >= tRPpb |
| tCKE | Duration of CKE high / low >= tCKE |
| tXP | Exit Power down to any valid command >= tXP |
| tXSR | Exit self refresh to any valid command >=tXSR |

# Real-Time Violations (Continued)

| Compliance parameter | Real-time compliance tests |
|---|---|
| **Additional LPDDR4 compliance parameters** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tCCD | READ -1 or any write (any bank) to READ-1 or any write (any bank) must be >= tCCD |
| tCCDMW | Any write to MASKED WRITE (same bank) must be > =tCCDMW |
| tRRD | ACTIVATE-2 to ACTIVATE-2 (different banks) must be >=tRRD |
| tMRW | MRW-2 to any valid command must be >= tMRW |
| tMRR | MRR-1 to any valid command must be >= tMRR |
| tRPab | PRECHARGE (all banks) to ACTIVATE-2/REFRESH (any bank) >= tRPab |
| tRPpb | PRECHARGE (per bank) to ACTIVATE-2 (same bank) or REFRESH (same bank or all banks) must be >= tRPpb |
| tXSR | Exit self refresh to any valid command >= tXSR |
| tPPD | Precharge (any bank to Precharge (any bank) must be >= tPPD |
| tRFCab | REFRESH (all banks to ACTIVATE-2 or REFRESH >= tRFCab |
| tRFCpd | REFRESH (per bank) to ACTIVATE-2 (same bank) or REFRESH > tRFCpb |
| tREFI | REFRESH command to REFRESH command must be <=tREFI*9 |
| tCKE | Duration of CKE high / low >= tCKE |
| tESCKE | Self Refresh Entry command to CKE low must be >= tESCKE |
| tCMDCKE | Any valid command to CKE low must be >= tCMDCKE |
| tCKEHCMD | Exit powerdown to any valid command >= tCKEHCMD |
| tMMRRIa | Exit powerdown to MRR >= tMRRIa (where tMRRIa = tXP (tCKEHCMD) + tMRRI) |
| BL16 | Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL16 |
| BL32 | Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL32 |
| BL OTF | Write/Read/Precharge - BL16 - Select these tests if your system uses Burst length OTF (on the fly) |
| MWtoP | MASKED WRITE-1 to PRECHARGE (same bank) >= MWtoP |
| MWtoR | MASKED WRITE-1 to READ (same bank) >= MWtoR |
| RFtoLAT | RD_FIFO to ZQCALLATCH >= RFtoLAT |
| RFtoLAT | RD_CALIBRATION to ZQCALLATCH >= RFtoLAT |
| RFtoLAT | MRR to ZQCALLATCH >= RFtoLAT |
| WFtoLAT | WR_FIFO to ZQCALLATCH >= WFtoLAT |
| WFtoLAT | MASKED WRITE-1 to ZQCALLATCH >= WFtoLAT |
| tZQCAL | ZQCALSTART to ZQCALLTACH >= tZQCAL |
| tZQLAT | ZQCALLATCH to any valid command >= tZQLAT |
| tZQRESET | ZQCALRESET to any valid COMMAnd >= tZQRESET |

## Post-process compliance violation analysis tool

The post-process compliance violation analysis tool automates state machine, protocol compliance, and protocol level bus cycle timing violation detection across Keysight logic analyzer traces. HTML reports of test results show margin details for both passing and failing tests.

Use the post-process compliance application tool to:

- Spot check logic analyzer traces for violations.
- Check logic analyzer trace captures leading up to system crashes for possible violations before the crash.

Post-process testing enables:

- Compliance violation testing across speed changes.
- "Click to" and "mark violation" features to quickly navigate from the compliance tool to violations in the traffic overview graph, waveform, or listing window.
- Margin information on each parameter to understand the range relative to the specification.

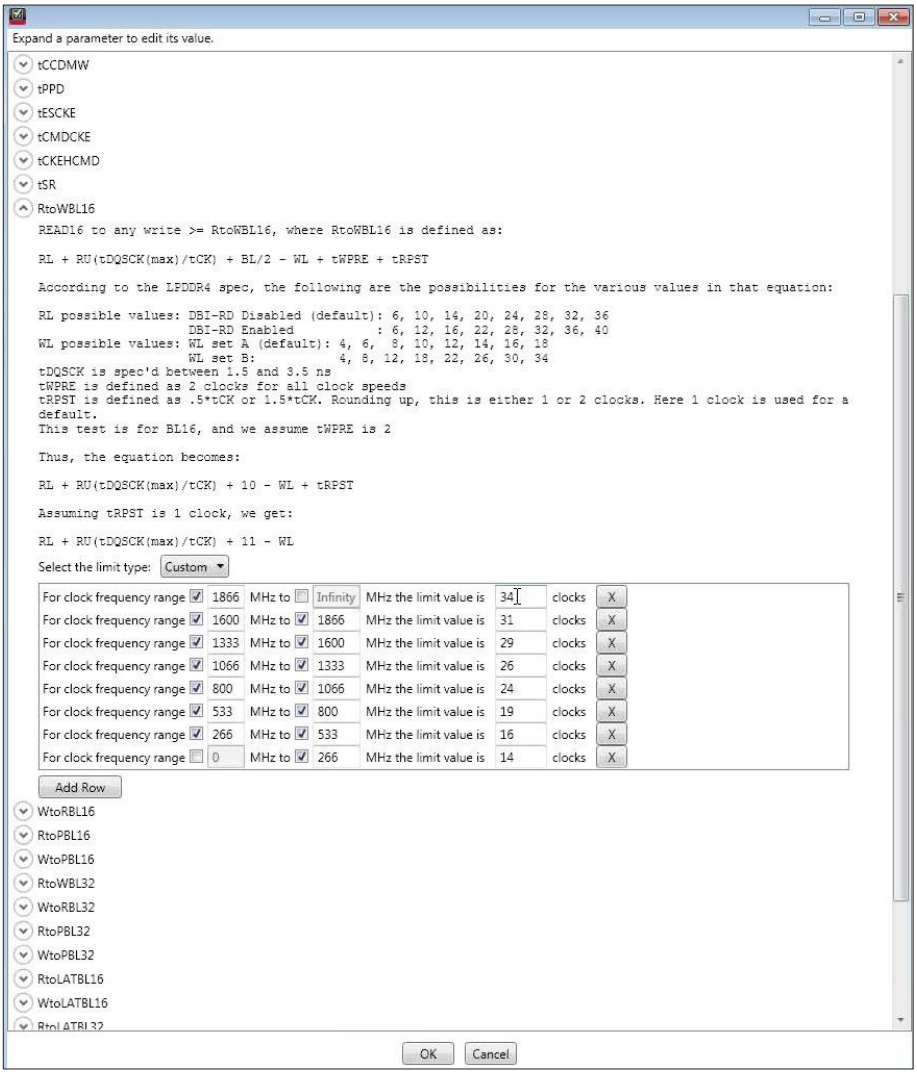



Figure 15. Speed ranges can be added in the post-process compliance tool for any parameter that has different criteria based on speed.

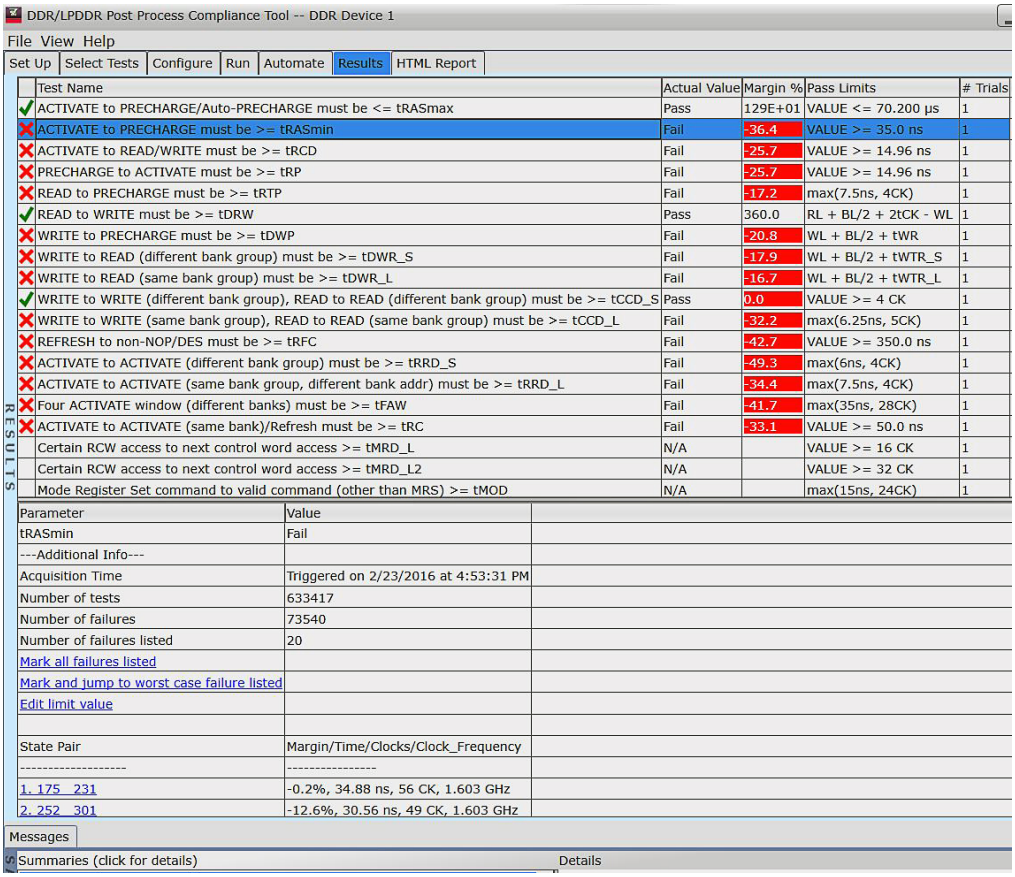



Figure 16. The post-process compliance tool includes hyperlinks to jump quickly to and/or mark violations and worst-case violations in the logic analyzer traces, transaction overview, and listing windows.

# Post Process Compliance Tests

| | |
|---|---|
| **State machine violations common to DDR, DDR2, DDR3, DDR4 and LPDDR, LPDDR2, LPDDR3, LPDDR4** | |
| READ to WRITE to an inactive row | |
| REFRESH to an active bank | |
| ACTIVATE to an active bank | |
| **Post-process violations** | |
| **Compliance parameter** | **Post-process compliance tests** |
| **Parameters common to DDR, DDR2, DDR3, and LPDDR** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRP | PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tDRW | READ to WRITE must be >= tDRW |
| tDWP | WRITE to PRECHARGE must be >= tDWP |
| tDWR | WRITE to READ must be > tDWR |
| tCCD | WRITE to WRITE, READ to READ must be >= tCCD |
| tRFC | REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC |
| tRRD | ACTIVATE to ACTIVATE (different banks) must be >= tRRD |
| tFAW | Four ACTIVATE window (different banks) must be>= tFAW |
| tRC | ACTIVATE to ACTIVATE (same bank) must be >= tRC |
| tREFI | REFRESH to REFRESH <= tREFI*9 |
| tMRD | MRS (Mode Register Set) to MRS must be >= tMRD |
| **Additional DDR3 compliance parameters** | |
| tZQoper | Long cal (normal operation) to valid command must be >= tZQoper |
| tZQCS | Short calibration (normal operation) to any valid command must be > tZQCS |
| tMOD | MRS (MODE Register Set) to valid command must be >= tMOD |
| tREFPDEN | REFRESH to power down entry >= tREFPDEN |
| tRDPDEN | READ to power down entry >= tRDPDEN |
| tWRPDEN | WRITE to power down entry >= tWRPDEN |
| tXPR | Exit RESET from CKE high to valid command >= tXPR |
| tXSDLL | Self refresh exit to valid command with DLL must be >= tXSDLL |
| tXPDLL | Exit precharge power down with DLL to any valid command < tXPDLL |
| **Additional DDR4 compliance parameters** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRP | PRECHARGE to ACTIVATE/PRECHARGE must be >= tRP |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tDRW | READ to WRITE must be >= tDRW |
| tDWP | WRITE to PRECHARGE must be >= tDWP |
| tDWR | WRITE to READ must be > tDWR |
| tCCD_L | WRITE to WRITE, same bank group must be >= tCCD_L |
| tRFC | REFRESH to valid command (non_NOP/DESELECT) must be >= tRFC |
| tFAW | Four ACTIVATE window (different banks) must be>= tFAW |
| tRRD_L | ACTIVATE to ACTIVATE (same bank group) must be >= tRRD_L |
| tRC | ACTIVATE to ACTIVATE (same bank) must be >= tRC |
| tREFI | REFRESH to REFRESH <= tREFI*9 |

# Post Process Compliance Tests (Continued)

| Compliance parameter | Post-process compliance tests |
|---|---|
| **Additional DDR4 compliance parameters (Continued)** | |
| tZQoper | Long cal (normal operation) to valid command must be >= tZQoper |
| tZQCS | Short calibration (normal operation) to any valid command must be > tZQCS |
| tMRD | MRS (MODE Register Set) to MRS must be >= tMRD |
| tMOD | MRS (MODE Register Set) to valid command must be >= tMOD |
| tREFPDEN | REFRESH to power down entry >= tREFPDEN |
| tRDPDEN | READ to power down entry >= tRDPDEN |
| tWRPDEN | WRITE to power down entry >= tWRPDEN |
| tXPR | Exit RESET from CKE high to valid command >= tXPR |
| tXSDLL | Self refresh exit to valid command with DLL must be >= tXSDLL |
| tXPDLL | Exit precharge power down with DLL to any valid command < tXPDLL |
| **Additional LPDDR2/3 compliance parameters** | |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tRTP | READ to PRECHARGE must be >= tRTP |
| tDRW | READ to WRITE must be >= tDRW |
| tDWP | WRITE to PRECHARGE must be >= tDWP |
| tDWR | WRITE to READ must be > tDWR |
| tCCD | WRITE to WRITE, must be >= tCCD |
| tRRD | ACTIVATE to ACTIVATE (different banks) must be >= tRRD |
| tFAW | Four ACTIVATE window (different banks) must be>= tFAW |
| tZQCL | Long calibration command to any valid command (or CKE low) must be > tZQCL |
| tZQCS | Short calibration command to any valid command (or CKE low) must be > tZQCS |
| tZQINIT | Init calibration command to any valid command (or CKE low) must be > tZQINIT |
| tZQRESET | Reset calibration command to any valid command (or CKE low) must be > tZQRESET |
| tMRW | MRW command to any valid command (or CKE low) must be > tMRW |
| tMRR | MRR command to any valid command (or CKE low) must be > tMRR |
| tREFBW | Greater than 8 REFRESH all bank commands in tREFBW |
| tREFW | Required number of refresh commands occur in time perion <= tREFW |
| tRFCab | REFRESH (all banks) to Active or Refresh must be > tRFCab |
| tRFCpb | REFRESH (per bank) to Activate (same bank) or REFRESH must be > tRFCpb |
| tRPab | PRECHARGE (all banks) to ACTIVE (any bank) must be >= tRPab |
| tRPpb | PRECHARGE (per bank) to ACTIVE (same bank) must be >= tRPpb |
| tCKE | Duration of CKE high / low >= tCKE |
| tXP | Exit Power down to any valid command >= tXP |
| tCKESR | Duration of self-refresh >= tCKESR |
| tDPD | Duration of power down to valid command >= tDPD |
| tXSR | Exit self-refresh to valid command >= tXSR |
| tXSR | Exit self refresh to any valid command >=tXSR |

# Post Process Compliance Tests (Continued)

| Compliance parameter | Post-process compliance tests |
|---|---|
| **LPDDR4** | |
| tRASmax | ACTIVATE to PRECHARGE/Auto-PRECHARGE must be <= tRASmax |
| tRASmin | ACTIVATE to PRECHARGE must be >= tRASmin |
| tRCD | ACTIVATE to READ/WRITE must be >= tRCD |
| tCCD | READ -1 or any write (any bank) to READ-1 or any write (any bank) must be >= tCCD |
| tCCDMW | Any write to MASKED WRITE (same bank) must be >= tCCDMW |
| tRRD | ACTIVATE-2 to ACTIVATE-2 (different banks) must be >= tRRD |
| tMRW | MRW-2 to any valid command must be >= tMRW |
| tMRR | MRR-1 to any valid command must be >= tMRR |
| tRPab | PRECHARGE (all banks) to ACTIVATE-2/REFRESH (any bank) >= tRPab |
| tRPpb | PRECHARGE (per bank) to ACTIVATE-2 (same bank) or REFRESH (same bank or all banks) must be >= tRPpb |
| tXSR | Exit self refresh to any valid command >= tXSR |
| tPPD | Precharge (any bank to Precharge (any bank) must be >= tPPD |
| tRFCab | REFRESH (all banks to ACTIVATE-2 or REFRESH >= tRFCab |
| tRFCpd | REFRESH (per bank) to ACTIVATE-2 (same bank) or REFRESH > tRFCpb |
| tCKE | Duration of CKE high/low >= tCKE |
| tESCKE | Self Refresh Entry command to CKE low must be >= tESCKE |
| tCMDCKE | Any valid command to CKE low must be >= tCMDCKE |
| tCKEHCMD | Exit powerdown to any valid command >= tCKEHCMD |
| tSR | Self refresh entry to self refresh exit >= tSR |
| tMMRRIa | Exit powerdown to MRR >= tMRRIa (where tMRRIa = tXP (tCKEHCMD) + tMRRI) |
| BL16 | Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL16 |
| BL32 | Write/Read/Precharge - BL16 - Select these tests if your system uses fixed BL32 |
| BL OTF | Write/Read/Precharge - BL16 - Select these tests if your system uses Burst length OTF (on the fly) |
| MWtoP | MASKED WRITE-1 to PRECHARGE (same bank) >= MWtoP |
| MWtoR | MASKED WRITE-1 to READ (same bank) >= MWtoR |
| RFtoLAT | RD_FIFO to ZQCALLATCH >= RFtoLAT |
| RFtoLAT | RD_CALIBRATION to ZQCALLATCH >= RFtoLAT |
| RFtoLAT | MRR to ZQCALLATCH >= RFtoLAT |
| WFtoLAT | WR_FIFO to ZQCALLATCH >= WFtoLAT |
| WFtoLAT | MASKED WRITE-1 to ZQCALLATCH >= WFtoLAT |
| tZQCAL | ZQCALSTART to ZQCALLTACH >= tZQCAL |
| tZQLAT | ZQCALLATCH to any valid command >= tZQLAT |
| tZQRESET | ZQCALRESET to any valid COMMAnd >= tZQRESET |

# Post Process Compliance Tests (Continued)

| Compliance parameter | Post process / Compliance tests |
|---|---|
| **LPDDR4** | **Refresh tests** |
| tREFI*9 | REFRESH command to REFRESH command must be <=tREFI*9 |
| tREFW | Required number of refresh commands occur in time period <= tREFW |
| tRFCab | Refresh (all banks) to Activate or Refresh must be > tRFCab |
| tRFCpb | Refresh (per bank) to Activate (same bank) or Refresh must be > tRFCpb |
| tREFI*2 | No more than 16 refresh commands occur in time period (tREFI *2) |
| | |
| **LPDDR4** | **Power down and self-refresh tests** |
| tXSR | Exit Self-Refresh to valid command >= tXSR |
| tXP | Exit power down to valid command >= tXP |
| tESCKE | Self-Refresh entry command to CKE low >= tESCKE |
| tCMDCKE | Any valid command to CKE low >= tCMDCKE |
| tCKEHCMD | Exit powerdown to any valid command >= tCKEHCMD |
| tSR | Self refresh entry to self refresh exit >= tSR |
| tMRRIa | Exit powerdown to MRR >= tMRRIa (tXP + tMRRI) |
| tCKE | Duration of CKE high/ low >= tCKE |
| | |
| **LPDDR4** | **Write/Read/Precharge/Cal - BL16 - Select these tests if your system uses fixed BL 16** |
| RtoWBL16 | READ16 to any write >= RtoWBL16 |
| WtoRBL16 | WRITE16 to READ16 >= WtoRBL16 |
| RtoRBL16 | READ16 to PRECHARGE (same bank) >= RtoRBL16 |
| WtoPBL16 | WRITE16 to PRECHARGE (same bank) >= WtoPBL16 |
| RtoLATBL16 | READ32 to ZQCALLATCH >= RtoLATBL16 |
| WtoLATBL16 | WRITE32 to ZQCALLATCH >= WtoLATBL16 |
| | |
| **LPDDR4** | **Write/Read/Precharge/Cal - BL32 - Select these tests if your system uses fixed BL 32** |
| RtoWBL32 | READ32 to any write >= RtoWBL32 |
| WtoRBL32 | WRITE32 to READ16 >= WtoRBL32 |
| RtoRBL32 | READ32 to PRECHARGE (same bank) >= RtoRBL32 |
| WtoPBL32 | WRITE32 to PRECHARGE (same bank) >= WtoPBL32 |
| RtoLATBL32 | READ32 to ZQCALLATCH >= RtoLATBL32 |
| WtoLATBL32 | WRITE32 to ZQCALLATCH >= WtoLATBL32 |
| | |
| **LPDDR4** | **Write/Read/Precharge/Cal - BL OTF - Select these tests if your system uses fixed BL OTF (on the fly)** |
| RtoWBL16OTF | READ32 to any write >= RtoWBL16OTF |
| WtoRBL16OTF | WRITE32 to READ16 >= WtoRBL16OTF |
| RtoRBL16OTF | READ32 to PRECHARGE (same bank) >= RtoRBL16OTF |
| WtoPBL16OTF | WRITE32 to PRECHARGE (same bank) >= WtoPBL16OTF |
| RtoWBL32otf | READ32 to any write >= RtoWBL32OTF |
| WtoRBL32OTF | WRITE32 to READ16 >= WtoRBL32OTF |
| RtoRBL32OTF | READ32 to PRECHARGE (same bank) >= RtoRBL32OTF |
| WtoPBL32OTF | WRITE32 to PRECHARGE (same bank) >= WtoPBL32OTF |
| RtoLATBL16OTF | READ32 to ZQCALLATCH >= RtoLATBL32OTF |
| WtoLATBL16OTF | WRITE32 to ZQCALLATCH >= WtoLATBL32OTF |
| RtoLATBL32OTF | READ32 to ZQCALLATCH >= RtoLATBL32OTF |
| WtoLATBL32OTF | WRITE32 to ZQCALLATCH >= WtoLATBL32OTF |

# LPDDR Decoder (B4661A-2FP/2TP/2NP)

Key features

- Decodes LPDDR, LPDDR2, LPDDR3 and LPDDR4 commands and MRS commands.
- Enables fast physical address trigger setup for LPDDR2/3.

Using the LPDDR decoder, valid read and write commands are decoded to include row and column addresses and the complete data burst associated with the command.

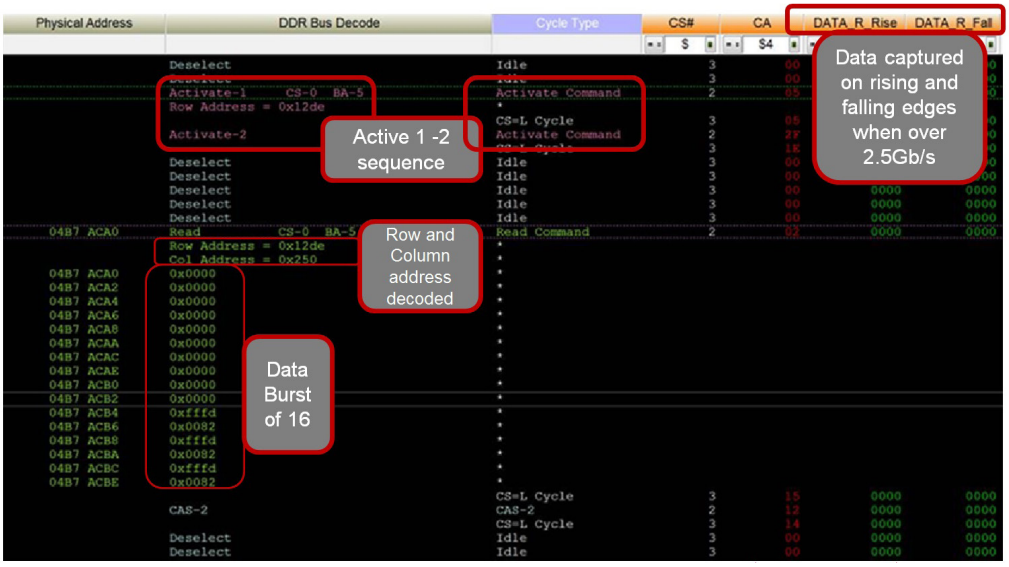



Figure 17. LPDDR4 decode in listing window.

## Physical address conversion tool in both DDR3/4 and LPDDR2/3 decoders with integrated trigger creation

Setting up a trigger on a specific physical address to obtain the corresponding data bus can be very tedious. The physical address trigger tool is included in the B4661A DDR decoder and LPDDR decoder options. The trigger tool allows you to automatically create a trigger on a specific physical address without having to go through a step-by-step trigger add-in. The physical address trigger tool incorporates a user-friendly interface to help the user quickly setup the trigger. DDR2/3/4 and LPDDR2/3 are covered by the physical address trigger tool. LPDDR4 is not covered by the physical address trigger tool.

# DDR Decoder with Physical Address Trigger (B4661A-1FP/1TP/1NP)

The B4661A DDR decoder covers DDR/2/3/4 and provides protocol decoding of memory transactions on traces captured using a Keysight logic analyzer. The protocol decoding software translates acquired signals into easily-understood colorized bus transactions showing associated data bursts for double-edge data rate captures.

Key features

- Decodes DDR, DDR2, DDR3 and DDR4 commands and MRS commands
  - Includes selection to decode MRS of DDR4 RDIMM and LRDIMM.
- Enables fast physical address trigger setup with physical address trigger tool.


Figure 18. DDR decoder display in listing window.

# B4661A Standard Software Features

# Standard Software Tools

## B4661A standard software features for DDR/LPDDR memory compliance testing and debug

- Default DDR probing configurations
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

# Default DDR Probing Configurations

Default configurations for Keysight DDR and LPDDR memory probes are available at no charge as part of the Keysight B4661A memory analysis software package. Default configurations include all labels and settings required to interface with the DDR setup assistant tool for rapid tuning of state mode measurements. Keysight default configurations include:

- Labeling and grouping of signals appropriate for each memory probe
- Symbol tables for command labels
- Trigger favorites for memory applications:
  - Basic trigger (simple read/write trigger)
  - Mode register settings (trigger to display mode register settings)
  - Filter NOPs (trigger to filter some of the NOPs)
  - Burst 4 write data (trigger to occur on a unique 4 burst write)
  - Burst 8 write data (trigger to occur on a unique 8 burst write)

# DDR Setup Assistant

## DDR measurements made fast, easy, and powerful

The DDR setup assistant simplifies measurement setup and minimizes the time to tune state mode measurements on the logic analyzer. DDR setup assistant guides you through even the most complex logic analyzer setup in minutes. It includes a variety of powerful, time-saving trigger features optimized for DDR measurements. The tool automatically configures optimum thresholds and controls DDR eye finder scans to rapidly locate optimal sample positions.

The DDR setup assistant tool is available at no charge as part of the Keysight B4661A memory analysis software package.

# DDR Eye Finder/Eye Scan

DDR eye scan makes it easy to determine the optimum acquisition sample point without requiring an oscilloscope. Qualified scans place the sample position at the center of the eye on every individual channel for maximum data capture reliability, including separate sampling positions for read and write data. Interface selections allow the user to customize scans for particular views and conditions of interest.

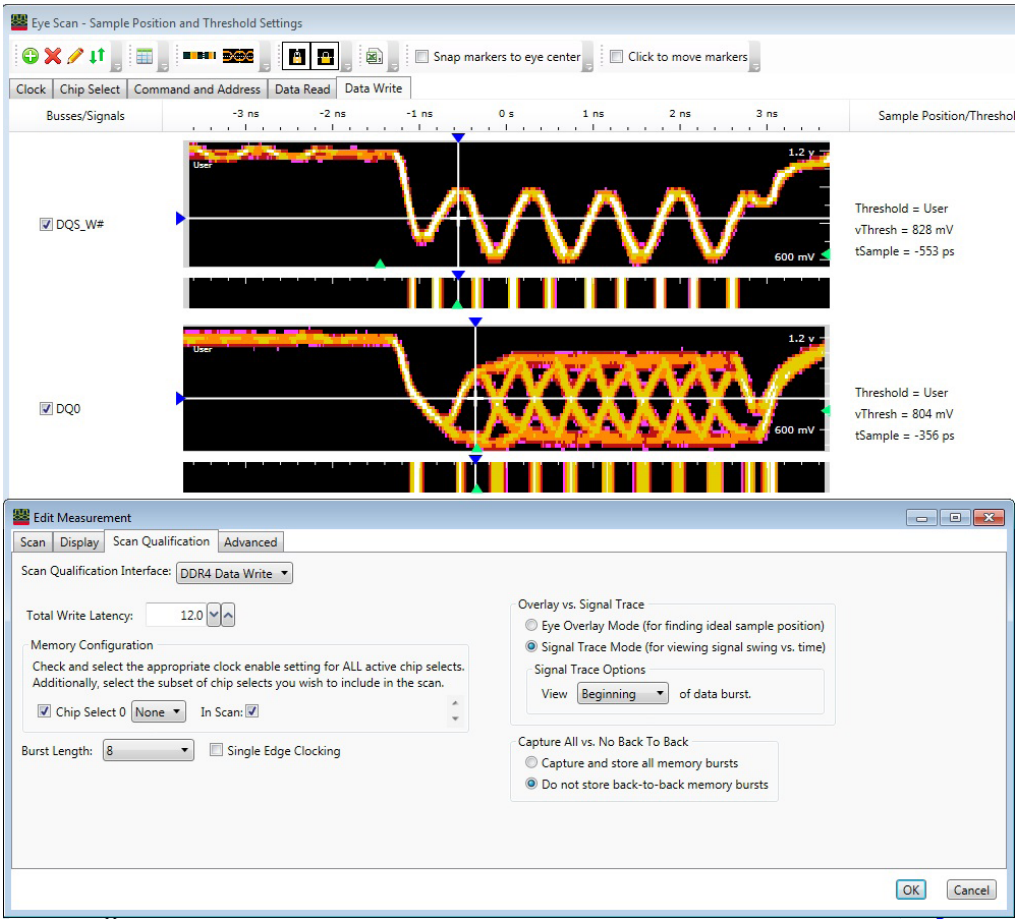



Figure 19. The DDR eye scan interface provides easy-to-follow pull-downs and options that control powerful scan qualifications for the user. Burst qualified eye scans from signal trace mode allow you to view the activity on the signals only when a burst is taking place. Screen shot above shows DDR4 2400 Mb/s read DQS and read DQ0 scanned in signal trace mode with no back-to-back bursts.

Increased insight decreases test time. Eye scan helps you identify bus level signal integrity and execution issues before you even take your first measurement by providing qualitative comparisons of eye diagrams relative to each other that allow you to quickly identify abnormalities at a glance.

Bus-level SI insight is the ability to view eye scans of up to hundreds of signals in a bus relative to each other. It is important because it provides:

- Quick, qualitative comparisons
  - Between signals in scan
  - Between scans where one variable has changed
  - More signals than possible on scope
- Powerful scan qualification provides views not easily obtained by any other method

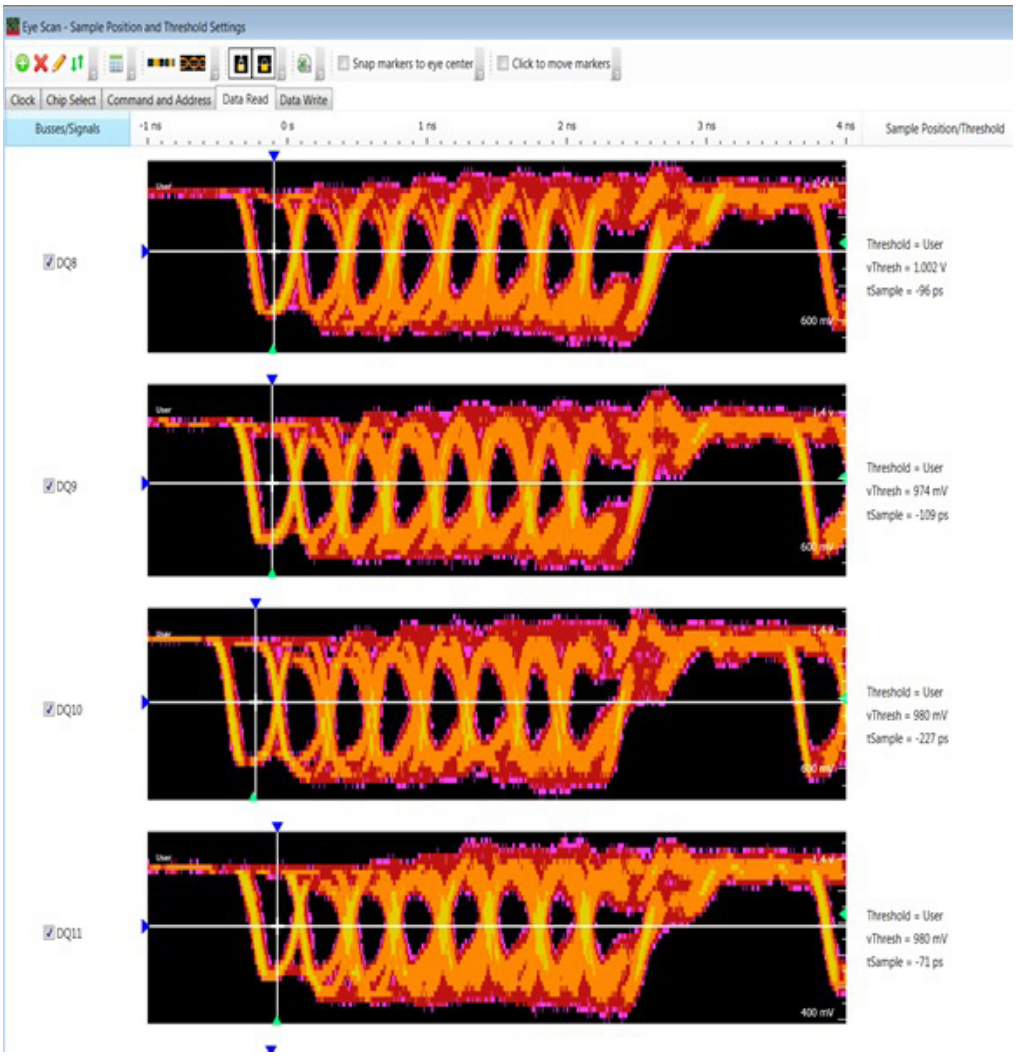



Figure 20. In this DDR4 at 3.1 Gb/s eye scan screen shot, scanned as read bursts with no back-to back transactions, using signal trace mode in DDR eye scan, we can quickly see that the first sample in the burst does not drive to the lowest value within the time of the first data sample. This indicates the possibility of Inter-Symbol Interference from either insufficient DRAM drive strength or incorrect termination settings.

# DDR Configuration Creator

The DDR/LPDDR configuration creator tool allows you to define the footprints layout per your custom probing solution used in the DDR/LPDDR setup and then create an XML configuration file based on your footprint information with the click of a button. The generated XML configuration file contains all the information for your custom probing required for the Keysight B4661A memory analysis software tools.

Once your custom XML configuration is created, it can be selected by the Keysight DDR setup assistant tool to define the DDR/LPDDR acquisition setup for your Keysight logic analyzer. By using a custom configuration file, you can ensure that the logic analyzer setup is correctly and completely set for a custom probing scenario.

## The DDR configuration creator tool enables

- Naming of footprints from schematic drawings.
- Tracking and highlighting which signals have already been assigned, helping to ensure that the user doesn't miss a signal or incorrectly double-assign a signal.
- Selection of either Soft Touch Pro footprints (three different schematic views) or custom (per pod) for signal assignments.

## Supported bus types

The DDR configuration creator tool can generate configuration files for the following DDR/LPDDR bus types.

- DDR3
- DDR4 (< 2.5 GHz and > 2.5 GHz clock rates)
- DDR5
- LPDDR2
- LPDDR3
- LPDDR4 (< 2.5 GHz and > 2.5 GHz clock rates)
- LPDDR5
- GDDR6 command/address

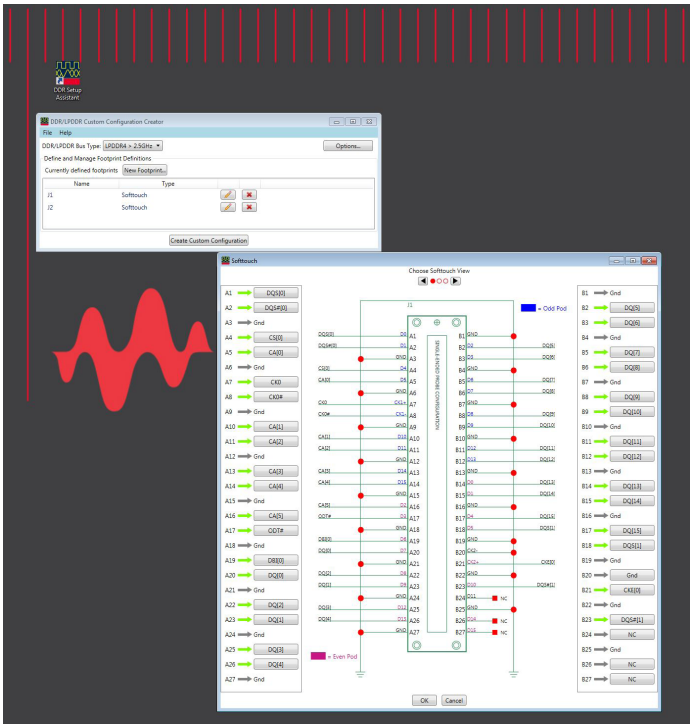


Figure 21. The DDR configuration creator tool lets you define Soft Touch Pro footprint or custom (per logic analyzer Pod) pin assignments.

# B4661A Memory Analysis Software Characteristics

## Logic Analyzer Compatibility

The B4661A memory analysis software is compatible with the following logic analyzer modules:

| Product | Description |
|---|---|
| U4164A | 136-channel 4 Gb/s state, AXIe-based logic analyzer module with ability to merge up to three modules |
| U4154B | 136-channel, 4 Gb/s state, AXIe-based logic analyzer module with ability to merge up to three modules |
| U4154A | 136-channel, 4 Gb/s state, AXIe-based logic analyzer module with ability to merge up to two modules |
| 16860A Series | Portable logic analyzers |

| Required state speed option | | U4164A base: 350 MHz clock | Option-700: 700 MHz clock | Option-01G: 1.4 GHz clock | Option-02G: 2.5 GHz clock |
|---|---|---|---|---|---|
| DDR/DDR2 | < 700 Mb/s | √ | √ | √ | √ |
| DDR3 | < 1400 Mb/s | | √ | √ | √ |
| | < 2500 Mb/s | | | √ | √ |
| | > 2500 Mb/s | | | | √ |
| DDR4 | < 2500 Mb/s | | | √ | √ |
| | > 2500 Mb/s | | | | √ |
| DDR5 | > 2500 Mb/s | | | | √ |
| LPDDR | < 700 Mb/s | √ | √ | √ | √ |
| LPDDR2 | < 1400 Mb/s | | √ | √ | √ |
| LPDDR3 | < 1400 Mb/s | | √ | √ | √ |
| | < 2500 Mb/s | | | √ | √ |
| LPDDR4 | < 2500 Mb/s | | | √ | √ |
| | > 2500 Mb/s | | | | √ |
| LPDDR5 | > 2500 Mb/s | | | | √ |
| GDDR6 | CA < 4000MT/s | | | | √ |

## Required Software

- Logic and protocol analyzer software
- B4661A memory analysis software

For best results, always download the latest version of the logic and protocol analyzer software from **www.keysight.com/find/LPA-SW-download**.

# B4661A Memory Analysis Software Includes

The logic and protocol analyzer software package combined with the B4661A installation package includes all standard and optional software. Standard features are always available for use. Optional features require the purchase of a license to enable the full functionality of the option. You can obtain a one-time, full-featured 30-day trial license from Keysight.com.

The Keysight B4661A memory analysis software provides four standard software features and four licensed memory analysis options.

## Standard software features

- Default configurations for DDR and LPDDR probing solutions for Keysight logic analyzers
- DDR setup assistant
- DDR eye finder/eye scan
- DDR configuration creator

## Licensed software options

- DDR decoder with physical address trigger tool (B4661A-1NP/1TP/1FP)
- LPDDR decoder with physical address trigger tool for LPDDR/2/3 (B4661A-2NP/2TP/2FP)
- DDR and LPDDR compliance violation analysis toolset (B4661A-3NP/3TP/3FP)
  - Post-process compliance violation analysis
  - Real-time compliance violation analysis
- DDR3/4, LPDDR2/3/4, and ONFi analysis (B4661A-4NP/4TP/4FP)

## DDR and LPDDR compatibility for B4661A options

| | DDR | DDR2 | DDR3 | DDR4 | DDR5 | LPDDR | LPDDR2 | LPDDR3 | LPDDR4 | LPDDR5 | GDDR6 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DDR decoder with physical address trigger tool (-1NP/1TP/1FP) | √ | √ | √ | √ | | | | | | | |
| LPDDR decoder (-2NP/2TP/2FP) | | | | | | √ | √ | √ | √ | | |
| DDR and LPDDR compliance violation analysis (-3NP/3TP/3FP) | √ | √ | √ | √ | | √ | √ | √ | √ | | |
| DDR3/4 and LPDDR2/3/4 performance analysis (-4NP/-4FP/4TP/4NP) | | | √ | √ | | | √ | √ | √ | | |
| DDR5 analysis and compliance (-5NP/5TP/5FP) | | | | | √ | | | | | | |
| LPDDR5 analysis and compliance (-6NP/6TP/6FP) | | | | | | | | | | √ | |
| GDDR6 analysis (-7NP/7TP/7FP) | | | | | | | | | | | √ |

# Ordering Information

## B4661A Memory Analysis Software

The B4661A installation package includes standard and optional licensed software. Standard features are always available for use. Optional licensed features require the purchase of a license to enable the full functionality of the option. You can obtain a one-time full featured, 30-day trial license from Keysight.com.

When ordering, if you request the email delivery option, you will be sent an electronic copy of the Entitlement Certificate so you redeem your license and begin using the software, often on the same day.

1. Select the desired license type

- Fixed perpetual license - the license is locked to the PC where the B4661A Memory Analysis software operates
- Transportable perpetual license - the license is locked to the PC where B4661A Memory Analysis software operates, however the license can be moved. The deletion from one host PC is confirmed prior to issuing a license for another host PC.
- Floating/server perpetual license - the license is locked to a license server from which the B4661A Memory Analysis software automatically checks out the necessary licenses. Licenses are checked back into the server once your analysis session is terminated. Each use of a licensed tool uses a single count of the server license. The count for each server license is:
  - B4661A-1NP server license count = 2
  - B4661A-2NP server license count = 4
  - B4661A-3NP server license count = 4
  - B4661A-4NP server license count = 4
  - B4661A-5NP server license count = 4
  - B4661A-6NP server license count = 4
  - B4661A-7NP server license count = 2

2. Select the desired functionality.

| | |
|---|---|
| B4661A | Memory analysis software for logic analyzers standard features at no-charge, includes: Default configurations, DDR setup assistant, DDR configuration creator, DDR EyeScan and EyeFinder |
| **Fixed perpetual licenses** | |
| B4661A-1FP | DDR listing decoder fixed perpetual license |
| B4661A-2FP | LPDDR listing decoder, fixed perpetual license |
| B4661A-3FP | DDR and LPDDR compliance violation, fixed perpetual license |
| B4661A-4FP | DDR3/4, LPDDR2/3/4, and ONFi analysis, fixed perpetual license |
| B4661A-5FP | DDR5 analysis and compliance validation, fixed perpetual license |
| B4661A-6FP | LPDDR5 analysis and compliance validation, fixed perpetual license |
| B4661A-7FP | GDDR6 analysis, fixed perpetual license |
| **Transportable perpetual licenses** | |
| B4661A-1TP | DDR listing decoder transportable perpetual license |
| B4661A-2TP | LPDDR listing decoder, transportable perpetual license |
| B4661A-3TP | DDR and LPDDR compliance violation, transportable perpetual license |
| B4661A-4TP | DDR3/4, LPDDR2/3/4, and ONFi analysis, transportable perpetual license |
| B4661A-5TP | DDR5 analysis and compliance validation, transportable perpetual license |
| B4661A-6TP | LPDDR5 analysis and compliance validation, transportable perpetual license |
| B4661A-7TP | GDDR6 analysis, transportable perpetual license |
| **Floating/server perpetual licenses** | |
| B4661A-1NP | DDR listing decoder network/floating perpetual license |
| B4661A-2NP | LPDDR listing decoder, network/floating perpetual license |
| B4661A-3NP | DDR and LPDDR compliance violation, network/floating perpetual license |
| B4661A-4NP | DDR3/4, LPDDR2/3/4, and ONFi analysis, network/floating perpetual license |
| B4661A-5NP | DDR5 analysis and compliance validation, network/floating perpetual license |
| B4661A-6NP | LPDDR5 analysis and compliance validation, network/floating fixed perpetual license |
| B4661A-7NP | GDDR6 analysis, network/floating perpetual license |

The B4661A operates with the following Logic Analyzers modules and probes from Keysight Technologies. Logic analyzer selection criteria includes: logic analyzer specifications and characteristics, maximum DDR technology data rate, and minimum data valid windows of the data eyes at the logic analyzer probe point.

| Product | Description |
|---|---|
| **AXIe-based logic analyzers** | |
| U4164A | 136-channel 4Gb/s state, AXIe-based logic analyzer module with ability to merge up to three modules. |
| U4154B | 136-channel, 4 Gb/s state, AXIe-based logic analyzer module allowing 3 modules to merge |
| U4154A | 136-channel, 4 Gb/s state, AXIe-based logic analyzer module |
| 16850A | Series Portable Logic Analyzers [1] |
| 16860A | Series Protable Logic Analyzers [1] |
| **DDR4 BGA interposers** | |
| W4633A | DDR4 x4/x8, 78 ball, ADD/CMD/DQ, 3.2Gb/s, BGA interposer for logic analyzers |
| W4643A | DDR4 x4/x8 78-ball, ADD/CMD/DQ, 3.6Gb/s, 2 wing, BGA interposer for logic analyzers |
| W4641A | DDR4 x16 96-ball, ADD/CMD/DQ, 3.6Gb/s, 2 wing, BGA interposer for logic analyzers |
| W4631A | DDR4 x16, 96 ball, ADD/CMD/DQ, 3.2Gb/s, BGA interposer for logic analyzers |
| W4636A | DDR4 x16, 96 ball, ADD/CMD/partial DQ, 2.4Gb/s, BGA interposer for logic analyzers |
| **DDR3 BGA interposers** | |
| W3631A | DDR3 x16 BGA command and data probe for logic analyzer and oscilloscope |
| W3633A | DDR3 x4/x8 BGA command and data probe for logic analyzer and oscilloscope |
| **Required software** | |
| Logic and protocol analyzer software. The latest logic and protocol analyzer software is available for download from **www.keysight.com/find/lpa-sw-download**. | |

For additional DDR/2/3/4/5 and LPDDR/2/3/4/5 probing options, contact your local Keysight representative **www.keysight.com/find/contactus** or refer to the U4164A Logic Analyzer Module - Data Sheet, 5992-1057EN.

Information on FuturePlus DIMM and SODIMM interposers for DDR2, DDR3, and DDR4 is available at **www.futureplus.com/DDR3-Memory/keysight-la-support-overview.html.**

For additional analysis software, refer to **www.keysight.com/find/logic-sw-apps.**

1. For DDR3 ADD/CMD analysis up to DDR3 1400 Mb/s (700 MHz clock).

## Related Literature

| Publication title | Pub number |
|---|---|
| *U4164A Logic Analyzer Module* - Data Sheet | 5992-1057EN |
| *U4154B Logic Analyzer Module 4 Gb/s State Mode* - Data Sheet | 5992-0108EN |
| *W4640A and W4630A Series DDR4 BGA Interposers for Logic Analyzers* - Data Sheet | 5991-4258EN |
| *16850 Series Portable Logic Analyzers* - Data Sheet | 5991-2791EN |
| *W3630A Series DDR3 BGA Probes for Logic Analyzers and Oscilloscopes* - Data Sheet | 5990-3179EN |
| *16860A series Portable Logic Analyzers* - Data sheet | 5992-1723EN |

## Learn more at: www.keysight.com

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